AD A137 394 ARMY DIGITAL TEST REQUIREMENTS ANALYTIC REPORT(U) 1/2
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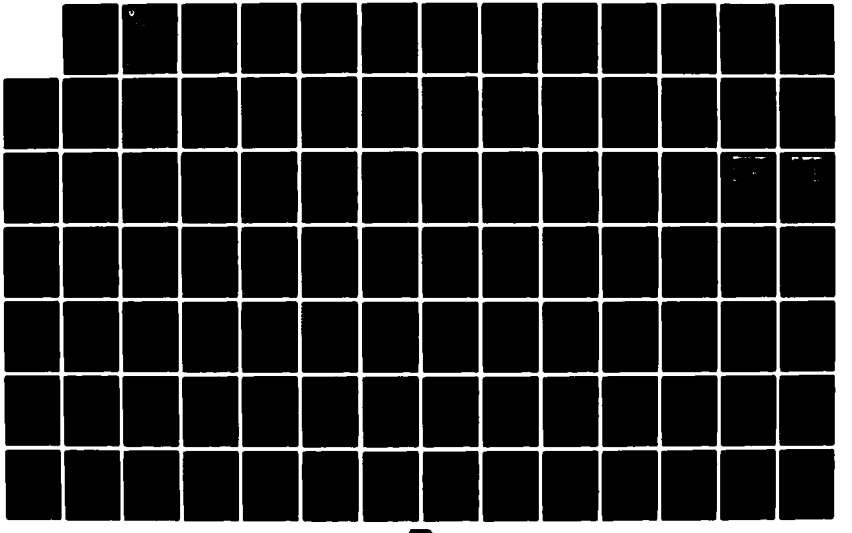

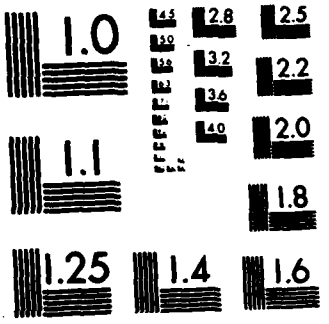

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RESEARCH AND DEVELOPMENT TECHNICAL REPORT
CECOM-80-0520-1

ARMY DIGITAL TEST REQUIREMENTS ANALYTIC REPORT

MANTECH INTERNATIONAL CORPORATION
2320 MILL ROAD
ALEXANDRIA, VIRGINIA 22314

JULY 1983

Final Report for Period Oct 1982 - July 1983

DISTRIBUTION STATEMENT
Approved for public release;
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PREPARED FOR:
US Army Test, Measurement and Diagnostic
Technology Laboratory

CECOM

US ARMY COMMUNICATIONS–ELECTRONICS COMMAND
FORT MONMOUTH, NEW JERSEY 07703

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REPORT DOCUMENTATION PAGE	READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER: CECOM-80-0520-1	2. GOVT ACCESSION NO.: AD-A137394
3. RECIPIENT'S CATALOG NUMBER	
4. TITLE (and Subtitle): ARMY DIGITAL TEST REQUIREMENTS ANALYTIC REPORT	5. TYPE OF REPORT & PERIOD COVERED: FINAL REPORT OCT 82 - JUL 83
6. PERFORMING ORG. REPORT NUMBER	
7. AUTHOR(s): W. Schmitt, M. Kelly	8. CONTRACT OR GRANT NUMBER(s): DAAK80-80-G-0520
9. PERFORMING ORGANIZATION NAME AND ADDRESS: ManTech International Corporation, 2320 Mill Road, Alexandria, Virginia 22314	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
11. CONTROLLING OFFICE NAME AND ADDRESS: USACECOM, Attn: DRCPM-TMDE-LS, Ft. Monmouth, NJ 07703	12. REPORT DATE: JULY 1983
	13. NUMBER OF PAGES: 37 plus appendices A thru D
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)	15. SECURITY CLASS. (of this report): Unclassified
	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

APPROVED FOR PUBLIC RELEASE, DISTRIBUTION UNLIMITED

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Automatic Test Equipment (ATE)
Built-In-Test (BIT)
Microprocessor (UP)

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

During the past decade, both the capabilities and technology of Army electronic equipment have rapidly advanced with the advent of microprocessor-based systems and complex VLSI chips.

The testing of these existing microprocessor-based systems/boards is presently straining the existing Army ATE assets in that expensive interface adaptors must be used for testing the microprocessor bidirectional data bus.

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ABSTRACT (continued)

Also, the digital pattern rate is at or above the upper limit of Army ATE and excessive test times are required because of limited bit pattern depth in existing Army ATE.

This report deals with an analytic approach taken to identify the analysis of the Army digital test requirements of the next 5-8 years (1988-1991). An envelope of digital technology parameters was developed after an analysis of data extracted from ten military systems, six commercial systems, trade journals, conferences, technical manuals and ATE industry surveys.

The report also addresses the premises that will be used to identify ATE requirements for the maintenance support of the present and future Army equipment. These premises will be used as a basis to generate a second report on ATE test requirements.

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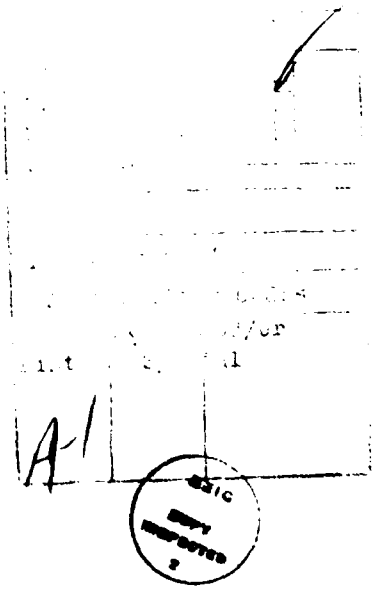
EXECUTIVE SUMMARY

This report is the first part of a two part report. The report outlines the analytic approach used for constructing the second report which is entitled "Army ATE Digital Test Requirements Report". The approach concentrated on developing the following three (3) major inputs:

(1) Digital System Data Base

A total of 33 circuit card assemblies (CCAs) and/or systems were selected for this survey. The cards/systems included processor, memory and interface types. The CCAs/systems surveyed were the following:

- o AN/PSG-2A (Communication Computer)
- o CP-1406/TYQ (Communication Computer)
- o Multiplexer TD-1236 (5 CCAs) (Communication)
- o PATRIOT (Weapon System)
- o XM-22 (Weapons Computer)
- o AN/AYK-14(V) (Airborne Computer)
- o MCF Super-Minicomputer, AN/UYK-41
- o MCF Micro Computer, AN/UYK-49
- o Single Module Computer for MCF Equipment
- o MLRS (10 CCAs) (Weapon System)
- o Intel Single Board Computer (Commercial)
- o Intel Bubble Memory (Commercial)
- o Intel 64K RAM (Commercial)
- o Intel DMA Controller (Commercial)
- o Intel Intelligent Communications Controller (Commercial)
- o IBM Disk Memory Set (5 CCAs) (Commercial)



(2) Digital Data analysis Results

Tables 1 and 2 found in the body of this analytic report summarize the digital data analysis that was carried out as part of the preparation for the Digital Test Requirements Report.

(3) Digital Technology/Testing Requirement Premises

Digital testing requirements of the future were determined based upon the following premises:

- Dynamic testing will be required for testing the new dynamic logic circuitry. The digital stimuli must be applied to hundreds of pins at rates well above the kilohertz range. The board tester will look more and more like the system environment, operating at full system, operating rate or even faster, to capture marginal faults.

- Digital pattern rates will increase to over 100MHz and clock rates will exceed 1 GHz. However, these capabilities will most likely not be implemented in military fielded systems in the 1988-1991 time frame.

- Digital stimulus/response pattern width will continue to trend towards longer data words, beyond 32 bits, before leveling off. Also, systems will be more bus-oriented thus reducing the number of random control and data signals required.

- Digital pattern depth will be influenced by memory bit density which will increase beyond 1 Mbit/chip by 1991.

- Data skew time will be dependent upon the minimum clock pulse width.

- Internal and external clock synchronization requirements will depend upon future design for testability implementation.

- Strobe delay requirements will decrease to well below 1 nSEC.

- Programmable stimulus/response voltage levels of the future will probably not exceed today's requirements. However, the lower voltages

will require finer resolution and accuracy. Maximum source and sink currents will decrease because of lower logic voltage levels and low fan-ins of bus oriented systems.

- Digital pulse rate requirements will increase, but built-in-test will be performing the really high speed testing. However, longer data burst length at system clock rates will be required for the future.

- Data and address word length will continue to increase, but more bi-directional I/O lines will be used, decreasing pin count. Also, military equipment will be more and more organized around serial and/or parallel data busses. This will likewise reduce pin counts.

- ATE programmable stimulus/response will need to be tri-state to handle bi-directional data busses of future military systems.

- Future ATE will require mixed programmable logic family capability in order to handle existing equipment that will still be around in the 1990s and special military equipment voltage levels for high-noise immunity logic.

- The advent of VLSI devices has made manual test pattern generation infeasible for most complex boards making some form of ATPG aid necessary.

1.0 INTRODUCTION

1.1 PURPOSE

The purpose of this report is to describe the analytic approach used to define the Digital Test Requirements for present and future Army Military equipment to direct advanced Army R&D efforts and to develop technical specifications for acquisition of Automatic Test Equipment (ATE).

1.2 OBJECTIVE

Historically, the capabilities and technology of Army digital equipment have advanced rapidly. In the past, this equipment development process did not adequately address the maintenance of new sophisticated equipment at the time of deployment. Consequently, inadequately equipped depots and other maintenance echelon were responsible for driving up maintenance costs.

The objective of the analytic approach was to outline the methods of data gathering/analysis and to state the premises that will be used in constructing the Digital Test Requirement Reports.

1.3 METHODOLOGY

In accordance with the above objective of this study, it was considered necessary that the analytic approach selected include the following considerations:

- Data sources from both the military and commercial domain should be used in order to provide the most recent knowledge and technology. The most advance military technology is often classified; therefore, commercial technology must also be used as a guide.

- An informal industrial technical survey should be performed regarding technology and ATE test requirements. Some future technologies and ideas are often not found in printed material because of industrial sensitivity.

- o A probability attribute should be assigned if possible to each of the future ATE test requirement as to when they will be a reality.

- o A digital parametric test requirement table should be developed around which a technical specification can be generated.

- o An investigation of ATE architectures should be conducted, and improvements should be suggested to guide the R&D efforts.

In view of the magnitude and objective of the project, the study was initially formulated to include the following tasks:

- Equipment/Digital Technology Identification
- Identification of Information Sources
- Data Collection
- Data Organization
- Data Review
- Special Research
- Technology Analysis
- Test Requirement Analysis (TRA)
- Test Requirement Premises

The approach used for each of these tasks is discussed in the following sections.

2.0 EQUIPMENT/DIGITAL TECHNOLOGY IDENTIFICATION

The purpose of this task was to define equipment types and digital technology that would be considered in detail during the study.

A list of representative unclassified military digital equipment was created for this study based on the judgement of a panel of ManTech International engineers. The Statement of Work (SOW) required that the list contain at least five (5) military equipments and that these reflect a reasonable sample of the present military equipment state-of-the-art in different equipment categories (i.e., communication, fire control, computer, etc.). The only equipment on the list that had been preselected by USACECOM was the Military Computer Family (MCF). After the list had been formulated, it was discussed with engineers at USACECOM to ensure that the list was not overly restrictive and was satisfactory.

A list of minimum digital technology parameters for analysis was also provided in the SOW by USACECOM. ManTech International's panel of engineers augmented the list to include what in their professional judgment would improve the projection of present and future digital test requirements. This list was then discussed with USACECOM engineers to ensure that it met their expectations and requirements.

3.0 INFORMATION SOURCES IDENTIFICATION

In order to make the Digital Test Requirement report data as comprehensive as possible, the following types of trade publications, papers and reports from both the Federal government and industry were reviewed:

- o Defense Technical Information Center Reports
- o Trade Journals
- o Related Studies
- o Technical Manuals/Specifications
- o Trade Conferences
- o ATE Industry Survey

The data gathered from all these sources will form the basis of the Digital Test Requirement report which will data base both the present digital test requirements and the possible future requirements in the 1988-1991 time frame.

3.1 DEFENSE TECHNICAL INFORMATION CENTER (DTIC)

This source of data is an information system containing technical reports under the auspices of the Department of Defense. DTIC provides a technical service by maintaining a data base of defense related reports including research studies that are submitted for distribution. Thus, it provides an excellent data source for information regarding military R&D efforts and technology.

The information center performs data searches for government and government contractors based upon a submitted topic/subject. The results are presented in the form of a directory with an abstract provided with each report title. A client simply reviews each report and determines which report he desires to order. For a minimal fee, the information center will provide a complete copy of any report requested.

The subject matter of these reports cover the entire spectrum of technical matter, for example, computers, microprocessors, digital testing, chemistry, physics, environ-ment, etc.

3.2 TRADE JOURNALS

Traditional industry journals such as Electronics, Electronic Design, Military Electronics, Test and Measurement World, and IEEE publications comprise this data source.

These journals often carry articles about digital technology and provide annual technology forecasts which were helpful with technical information. The journal articles provide the most current source of technical data, since books and reports often become dated in a short time after publication because of the rapid advances being made in digital technology.

3.3 RELATED MANTECH STUDIES/REPORTS

Since ManTech has performed many other similar studies under contract, a review of prior ManTech contracts in allied area was conducted to determine if any material in those reports could be helpful. In particular, ManTech reports on microprocessor test program generation and digital simulation were utilized.

3.4 MILITARY MANUALS/SPECIFICATIONS

In the area of military equipment technology and test requirements, two important data sources were military technical manuals and equipment specifications.

Technical manuals proved to be the most useful because they contained such equipment information as operational description, function description, functional block diagram, schematics and parts list, which are essential to determining equipment digital technology and test requirements. However, because of the time lag in generating these manuals, they were an important information source only for military equipment developed in the 1970s.

For contemporary equipment or equipment under development, it was found that equipment design specifications were the main and often the only sources of information. These specifications usually provide data about the general performance requirements of military equipment and therefore do not have the detailed information of

the technical manual. However, they provide some insight into the equipment technology and functional capabilities.

3.5 TRADE CONFERENCES

Trade conferences have been excellent sources of information for digital technology, built-in test, and ATE test program development techniques. The various trade meetings organized by the IEEE have been a particularly useful source of technical papers and reports in the past. Consequently, a necessary step in the preparation of this report was to select appropriate trade conferences that would provide pertinent data in the areas mentioned.

3.6 ATE INDUSTRY SURVEY

Another approach used in constructing the technical report for obtaining advance digital technology projection and ATE test program development advance methodologies was the conducting of informal surveys at trade conferences and ATE user meetings. This was in addition to using our own past and present experience with both government and commercial TPS clients.

An informal survey was targeted toward a selected cross section of current digital ATE users and suppliers. This community was selected for the survey in order to assess their opinions and thoughts relative to both present and future requirements for digital ATE based upon the detail knowledge of the ATE marketplace and technology.

4.0 DATA COLLECTION

After the identification of the data sources, the arduous task of collecting the pertinent data was initiated. The approach taken with each of the data sources to acquire information is described below.

4.1 DEFENSE TECHNICAL INFORMATION CENTER (DTIC)

4.1.1 TECHNOLOGICAL SEARCH PROCESS

Since the data base provided by the DTIC is enormous, it was initially necessary to narrow down the search by selecting pertinent topics which might provide data for the purpose of constructing the Digital Test Requirements Report. The topics selected were microprocessors, digital testing methods, VSHIC, digital computers and digital systems. A search was conducted for the years 1977 to the present.

The result was a listing that contained a list of relevant reports and related abstracts.

4.1.2 REPORT SELECTION PROCESS

The listing supplied by DTIC was reviewed by reading the abstracts to determine which reports warranted further investigation. The investigation then involved ordering copies of the pertinent reports and reviewing them to select those that would be relevant to the construction of the Digital Test Requirements Report. The bibliography (Appendix A) lists the reports selected.

4.2 TRADE JOURNALS

4.2.1 SEARCH

The search effort began with acquiring issues of the following trade journals from 1976 to the present:

- Electronic Design
- Electronics
- Mini-Micro Systems
- Electronic News

- o Electronic Test
- o IEEE Computer
- o EDN
- o Computer Design
- o Digital Design
- o Electronic Products
- o Defense Electronics
- o Military Electronic
- o Electronic Component News
- o Test and Measurement World

4.2.2 ARTICLES SELECTION

A panel of engineers selected those articles which were germane to the Digital Test Requirements report. The articles were chosen on the basis of their relevancy to the following subjects:

- o Digital Technology Forecast/R&D Efforts
- o Digital Testing
- o Military VHSIC Program
- o New Digital Components
- o Microprocessors and Microprocessor Peripherals
- o Digital Busses
- o Microprocessor Based Systems
- o Built-in Test
- o ATE Technology/Requirements
- o ATE Test Program Development Techniques
- o Test Program Development ACPS
- o Artificial Intelligence

The articles that were selected are listed in the bibliography, Appendix A.

4.3 COMPANY RELATED STUDIES/REPORTS

4.3.1 SEARCH

This effort involved a review of all previously contracted ManTech studies and reports dating back to 1975.

4.3.2 STUDIES/REPORTS SELECTION

ManTech studies/reports to be used in this effort were selected on the basis of whether they were germane to any of the following technical areas:

- o Digital Technology
- o Built-in-Test
- o ATE Technology
- o ATE Test Program Set Development
- o ATE Test Program Set Development Tools
- o Microprocessor Testing
- o Technology Impact on Testing

The company studies/reports selected can be found in the bibliography in Appendix A under ManTech related studies/reports.

4.4 MILITARY TECHNICAL MANUALS/SPECIFICATIONS

4.4.1 TECHNICAL MANUAL INDEX REVIEW

The Army technical manual index was reviewed for selection of candidates for military equipment to be used in the technical report.

4.4.2 IDENTIFICATION OF TECHNICAL MANUAL/SPECIFICATION SOURCES

The main sources for technical manuals on electronic equipment were identified as the military libraries at the Pentagon, Army Personnel offices in Alexandria, Virginia (Hoffman Building) and Ft. Monmouth in New Jersey. The Army's TMDE Labs were the main source of data for MCF and Multiplexer TD 1236.

An excellent data source for the military equipment specifications used in the technical report proved to be the data packages used on other ManTech contracts which pertained to test requirement analysis. These data packages often contained all or part of the following data: specification, schematic and parts list. Our Huntsville, Alabama office was particularly helpful in this regard since they have supported for a number of years a large number of MICOM ATE related activities.

4.4.3 TECHNICAL MANUAL/SPECIFICATION ACQUISITION AND REVIEW

The military libraries were visited and technical manuals were selected as possible data sources. The selected manuals were borrowed from all three libraries for closer review to determine if the equipment selected was qualified to be included in the study data base.

4.4.4 SELECTION PROCESS

The selection of military equipment to be included in the technical report was dependent upon the availability of data and the need to include a variety of digital systems used in different military applications such as weapon systems, aviation, tactical and strategic communication. An additional consideration was whether the digital systems represented a valid sample of military digital technology from 1970 to the present.

The final judgment of whether a military equipment was to be selected was based upon its meeting one or more of the following digital technical criteria:

- Microprocessor Technology Utilized
- Circuit Complexity Includes LSI
- Logic Family TTL or Later Technology
- Bus Architectural Utilization
- Built-in Test Implementation

The military digital systems selected for analysis based upon the above criteria are listed in paragraph 9.2.

4.5 TRADE CONFERENCES

4.5.1 IDENTIFICATION OF APPLICABLE CONFERENCES

Annually, over the years, excellent papers have been presented and panels held at the Cherry Hill Test Conference, AUTOTESTCON, and the ATE Seminar/Exhibit. These test

conferences have been, in our judgment, a high quality source of advanced technological information. Consequently, these test conferences were selected as data sources for the construction of the technical report.

One additional new conference sponsored by the Data Processing Management Association (DPMA) called "Computer In Defense" was also selected. At this conference seventeen (17) leading experts from Army, Air Force, NASA and industry lead the conference and showed their knowledge pertaining to the problems of designing and maintaining embedded computer systems, including the MCF, for today and the 1990s.

4.5.2 SELECTION OF CONFERENCES

At the two day "Computer in Defense" conference, the presentations in the following technological areas were chosen as relevant to this digital requirements study:

- Very Smart Weapons
- Artificial Intelligence
- MCF
- Potential Supercomputer Architectures
- Mass Storage and Access-trend
- Built-in- Test for Future Generations
- Programmer-less Software Generation
- System Development Aids and Methodology
- The Next Ten Years and Beyond

At the Cherry Hill Conference, presentations were attended on the following subjects:

- Board Test
- Self Test
- Memory Test
- Microprocessor and VLSI Test
- Computer-Aided Test
- Test Software
- Design for Testability

4.5.3 SURVEY OF ATTENDEES

While attending the above National conferences, the time between presentations was used for informal conversation with other attendees to obtain their opinion regarding the following topics:

- o Microprocessor-Based System Testing
- o Future ATE Requirements
- o Digital Technology Advances
- o ATE Test Program Development Aids

These opinions were integrated with the ATE industry survey results, and the results are summarized in the "Army Digital Test Requirements Report."

4.5.4 PROCEEDINGS

Proceedings of the Cherry Hill, AUTOTESTCON and ATE Seminar/Exhibit conferences were reviewed for content pertinent to the technical report on Digital Test Requirements. Examples of the type of subject matter considered pertinent were as follows:

- o Microprocessors
- o Built-in-Test
- o Microprocessor-Based Systems
- o Automatic Test Program Generators
- o Digital Simulators
- o Testing Methods
- o General Digital Technology

4.6 ATE INDUSTRY SURVEY

4.6.1 ATE USERS/MANUFACTURERS SURVEYED

A key method used for obtaining data regarding advanced digital technology projections and ATE test program development techniques was the conducting of

informal surveys. Surveys were conducted at a GenRad ATE user meeting and during plant visits to the test departments of major manufacturing divisions of ITT and IBM. Our own ATE experience with the following past and present government and commercial clients has also been included as part of the survey:

- o NAVSEA
- o STEEP Program
- o NAVELEX ATE Programs
- o AEGIS Program
- o NAVAIR ATE Programs
- o IBM
- o ITT
- o Harris
- o TRW
- o Westinghouse

4.6.2 TYPE OF SURVEY

Over the years, many approaches for obtaining opinions and judgement have been devised. These include telephone polling, mailed questionnaires and personal interviews. It has been our experience that telephone polling is too impersonal a technique. Mailing questionnaires to be filled in by respondents even (those who agreed ahead of time) often creates problems. The questionnaires are not returned in a timely fashion, if they are returned at all. In addition, there is always a certain degree of ambiguity associated with the written questions. Also, most significantly, it is never possible to anticipate all the areas a respondent may believe are important and may want to discuss. In other words, the written questionnaire cannot be sufficiently flexible for all respondents.

Therefore, for this report, we chose to employ informal, personal, anonymous (so interviewee can speak candidly) interviews to solicit opinions and judgements from persons representing diverse viewpoints on a given topic. This technique has been used over the last decade in many studies for governmental and industrial organizations. These personal interviews offer flexibility and are time saving compared to the questionnaire method.

4.6.3 PROCEDURE

Sixteen (16) informal anonymous interviews were conducted regarding digital technology, ATE test requirements and ATE test software tools. The interviewees were chosen from the following sources:

- o GenRad User Meeting Attendees
- o Past and Present Clients
- o Trade Conference Attendees
- o ManTech Personnel

The people selected were individuals whose expertise in the area of digital technology and ATE software development was established by their participation in a trade conference or by their job experience/responsibilities.

The purpose of the interviews was to gain insight into how the ATE industry expected the digital technology, digital test requirements, and ATE test software development requirements/methodology would evolve over the next 5-8 years.

The informal inteviews were conducted as follows:

- o The interviewees were asked to evaluate digital technology parameters devised from a careful literature review and the SOW, in terms of their importance. They were also asked to list any additional parameters they felt were important.

- o The interviewees were then asked to project the evolution of each digital parameter over the next decade.

- o Then, they were asked on what assumptions their projections were based.

- o They were asked to name digital technology drivers and what effect they will have on ATE test requirements.

- They were asked for any pertinent comments.

The result of this survey is summarized and integrated with the other data in the "Army Digital Test Requirements Report."

5.0 DATA ORGANIZATION

5.1 DATA CATEGORIES

All material received was designated as belonging to one of two (2) categories - commercial or military data. The definition upon which the assignment was based was as follows:

- o Commercial Data Sources
  - — Conference Publication
  - — Commercial Trade Journals
  - — ATE Industry Survey
  - — Technical Papers
  - — Cherry Hill Test Conference
  - — Commercial Catalogues
- o Military Data Sources
  - — Technical Manuals
  - — Military Specification
  - — Military Schematic/Part Lists
  - — Company's previous Military Report
  - — Military Electronic Magazine
  - — "Computer In Defense" Conference

5.2 PERTINENT DATA SELECTION/RECORDING

Once the data was categorized as commercial or military, the individual data item was reviewed and pertinent passages/paragraphs were identified. The resulting pertinent data was then recorded by data item, title, author and page numbers. This was used to form a data base which served as the report bibliography (Appendix A).

6.0 DATA REVIEW

6.1 COMPREHENSIVE REVIEW

With the data base now being organized and recorded, the process of a comprehensive data review was made possible. The review consisted of verifying coverage of the following key digital parameters and technologies which are incorporated into the data base:

- o Microprocessor Data Bus Bit Density
- o Microprocessor Clock Frequencies Ranges
- o Microprocessor Clock Synchronization and Controllability
- o Microprocessor Instruction and Machine Cycle Time
- o Microprocessor Memory Addressing Capability
- o Microprocessor BIT
- o Microprocessor Testability Attributes
- o Microprocessor General Testing Consideration
- o Memory Types
- o Memory Size
- o Memory Data and Address Lines Quantity
- o Memory Access Time
- o Dynamic Memory Refresh Rate
- o Memory General Testing Considerations
- o Interface Bus Types
- o Bus Architecture (Format, Control, Data Width, etc.)
- o Digital Test Methods
- o Digital Test Software Development Methods
- o Digital Test Software Development Tools
- o Artificial Intelligence
- o Test Program Generation Techniques

6.2 REVIEW CONCLUSIONS

The data base was found to be generally sufficient. However, in some cases, the documentation of military systems, particularly the MCF, lacked sufficient detail at

the circuit card level to perform detailed test requirements analysis. In order to fill the void caused by the lack of detailed digital design data, commercial printed circuit cards, which performed similar functions to cards in the military systems (for which insufficient data was available), had to be identified and analyzed. Great care was taken to ensure that the substituted "commercial equivalents" employed "similar to" technology and had a similar level of complexity of the target military circuit card assemblies.

7.0 SPECIAL RESEARCH

As mentioned in the previous section, commercial counterparts to military equipment had to be identified to obtain the required data to perform test requirement analysis.

In cases where card level data existed, the specific digital components in the military/commercial equipment part list needed to be supplemented with their individual specifications to generate a comprehensive test requirement analysis.

The type of data sources selected for this phase of the analysis were as follows:

- IC Master
- National Semiconductor catalogs
- Intel Catalogs
- TI Data Books
- Osborne's Introduction to Micro-computers Volumes 1, 2, and 3
- DATAPRO

8.0 TECHNOLOGY ANALYSIS

8.1 COMMERCIAL TECHNOLOGY

In order to assess the effects of current and projected developments in digital integrated circuits on the Army's TMDE requirements, it is necessary to look at the present state of commercial digital circuit technology and its expected progress in the near future. The areas of digital circuit technology studied and analyzed include the following:

- o Bipolar Devices
  - — TTL
  - — Schottky TTL
  - — Integrated Schottky Logic (ISL)
  - — Schottky Transistor Logic (STL)
  - — Integrated Injection Logic (I^2L)
  - — ECL
- o MOS Devices
  - — PMOS
  - — NMOS
  - — Bulk CMOS
  - — HMOS
  - — CMOS/SOS
- o Developmental Devices
  - — Gallium Arsenide (GaAs)
  - — Josephson Junction

In addition, the impact of improvements in lithography and circuit etching was also evaluated.

8.2 MILITARY TECHNOLOGY

In the area of military equipment technology, this portion of the study focused on the VHSIC program. Phase 1 of the VHSIC program, scheduled for completion in 1986, comprises six efforts employing bipolar, NMOS and bulk CMOS technologies. The effects of this program were analyzed, along with the effects of commercial digital technology developments, to project future Army TMDE requirements regarding:

- o Operating speeds
- o Voltage levels
- o Memory requirements (depth, width and speed) for stimulus and response
- o Effects of built-in-test (BIT).

The study takes in the Military Computer Family (MCF) and a range of Army digital equipments currently in production. This portion of the study is discussed under Test Requirements Analysis.

8.3 TEST PROGRAM SET (TPS) DEVELOPMENT APPROACHES AND TOOLS

In addition to assessing the impact of advancing digital circuit technology on ATE hardware, the Digital Test Requirements study considers the implications of VLSI and VHSIC devices with regard to TPS development and the tools used therein. Based upon our analyses the topics that need to be addressed are the following:

- o Manual TPS Generation
- o Capabilities and Limitations of Existing Simulators and ATPGs
- o Possible Improvements in Simulators and ATPGs
- o Application of CAD/CAM to TPS Development
- o Artificial Intelligence (AI applied to TPS)
- o Heuristic Programs
- o Programs with teaching capability
- o Effects of BIT on test program sets.

9.0 TEST REQUIREMENTS ANALYSIS (TRA)

9.1 TRA DOCUMENTATION

To establish a baseline of current digital test requirements, normalized data entry forms were developed and used to record the characteristics of a representative sample of military and commercial systems/circuit cards. The parameters tabulated on these forms include data and clock rates, voltage levels, I/O pin counts, serial and parallel data busses, dynamic testing requirements, and serial and parallel word length/depth requirements.

9.2 TRA CANDIDATES

A total of 33 circuit cards and/or systems were selected for this study. The candidates included processor, memory and interface technology. The equipments selected were the following:

- AN/PSG-2A (Communication Computer)
- CP-1406/TYQ (Communication Computer)
- Multiplexer TD-1236 BITE CCA (Communication)
- Multiplexer TD-1236 Microcontroller (Communication)
- Multiplexer TD-1236 Group Mux/Demux (Communication)
- Multiplexer TD-1236 Timing CCA (Communication)
- Multiplexer TD-1236 Super Group (Communication)
- Patriot (Weapon System)
- XM-22 (Weapon Computer)
- AN/AYK-14(V) (Airborne Computer)
- MCF Super-Minicomputer, AN/UYK-41
- MCF Microcomputer, AN/UYK-49
- Single Module Computer for MCF Equipment
- MLRS Controller and Memory Interface (Weapons Systems)
- MLRS Central Processor Unit (Weapons Systems)
- MLRS Fuze Setter (Weapons Systems)
- MLRS Volatile RAM (Weapons Systems)
- MLRS Symbol Generator (Weapons Systems)
- MLRS CPU Interface (Weapons Systems)
- MLRS Memory Control (Weapons Systems)

- o MLRS Non-volatile RAM (Weapons Systems)
- o MLRS Communications Controller (Weapons Systems)
- o MLRS ROM (Weapons Systems)
- o Intel Single Board Computer (Commercial)
- o Intel Bubble Memory (Commercial)
- o Intel 64K RAM (Commercial)
- o Intel DMA Controller (Commercial)
- o Intel Intelligent Communications Controller (Commercial)
- o IBM MPA1 (Commercial)
- o IBM MPA2 (Commercial)
- o IBM Host Adapter Fast (Commercial)
- o IBM Host Adapter Slow (Commercial)
- o IBM Read/Write Control (Commercial)

The TRAs for these cards are included in Appendix B.

9.3 DEVELOPMENT OF DIGITAL TEST REQUIREMENTS

The digital data technology baseline envelope developed in Table 1 is based partly on the Test Requirements Analysis for existing Army digital equipment and partly on a study of recent developments in commercial digital hardware. Typically, military application of advanced technology has lagged behind commercial developments because of the time-consuming process of qualifying new devices for military use under MIL-STD-883 and MIL-M-38510. This situation will likely change, however, as the VHSIC program begins to produce results. The VHSIC program encompasses (36) four competing technologies - bipolar, NMOS, bulk CMOS and CMOS/SOS and involves six contractors working on the designs of 33 integrated circuits. To date, two devices, a 25MHz matrix switch (37) and an 80 MHz digital correlator (28), have been announced, and devices with 100 MHz clock rates are anticipated.

The Military Computer Family (MCF) comprises the AN/UYK-41 super-minicomputer, the AN/UYK-49 microcomputer and a single module computer. Preliminary specifications for these machines are summarized in Appendix C, and their important characteristics appear in Table 1. MCF units are intended to be supported by the AN/USM-410 (EQUATE) and/or the AN/USM-465 (GENRAD 2225) ATE systems, supplemented by built-in-test (50). If this is achieved the impact of the MCF on future Army

ATE requirements will be minimal. However, if the requisite level of fault isolation by BIT is not attained, contingency planning must be initiated and the MCF must be considered in formulating requirements for future ATE.

Currently, the highest-speed logic family in widespread use is ECL. Among the most advanced devices in this family are the Motorola MC 10900 series bit-slice microprocessors, with a clock rate of 50 MHz (11), and the MC 10 H145, a RAM with an access time of 3 nSec (32). Because of its high power consumption, ECL is not expected to be a major factor in the future of digital circuit development.

The technology which has yielded the largest scale integrated devices is NMOS. This family has produced the Intel iAPX-432, the first 32 bit microprocessor (23) and the HP 9000 series, another 32 bit machine with an instruction cycle time of 165 nSec and a data transfer rate of 6M bytes/second (23, 30).

The most promising technologies for the future appear to be CMOS/SOS and Ga As. After several years of relative inactivity, new developments in CMOS/SOS have recently been announced by Hughes (the 80 MHz correlator mentioned above), HP (a three-chip, 64 bit, floating point calculator set, operating at 12 MHz) (13) and RCA (EPIC family of radiation - hardened devices, including an 8-bit slice operating at 10 MHz) (23).

Most laboratory developments of GaAs digital integrated circuits have been announced by Japanese firms (12). However, TI, HP, and Lockheed have made some progress in this field (12). GaAs technology is not utilized in the VHSIC program, but DoD recently revealed a program to partially fund GaAs pilot production facilities for memories and gate arrays (34). GaAs shows the greatest potential for producing ICs operating in the gigahertz range (10).

Table 2 lists salient characteristics of some widely used data busses. Of these, the most important for military applications is the MIL-STD-1553 bus, which is a Manchester II type biphase code. The advantages of this bus are the following:

- o single, shielded, twisted-pair transmission line
- o self clocking
- o no dc component - allows ac coupling

Table 1. Digital Data Technology Envelope

Technology Area	Parameter	Range		Notes
		Military Data Base	Commercial Data Base	
Microprocessor	Clock Frequency	614KHz to 2MHz	100KHz to 50 MHz (11)	Military uP Types 2901, 9900, 9080, Z80
	Data Rate (bits/sec)	.6Mb/s* to 6Mb/s	.1Mb/s* to 6Mb/s (30)	*Estimated
	Word Length	2 to 16 bits	2 to 32 bits (86, 23)	
	Instruction Cycle Time	1.6uSec to 15uSec	165nSec to 5uSec (30, 86)	
	Memory Size (bytes)	1K to 32K	1K to 16M (86, 10)	
RAM	Access Time	60nSec to 220nSec	3nSec to 900nSec (32, 86)	
	Bits/Chip	1K to 4K	1K to 64K (86)	
ROM	Access Time		45nSec to 10uSec	No military example found in Data Base
	Bits/Chip		1K to 1M (86,33)	
PROM/EPROM	Bits/Chip	2K to 16K	1K to 128K (86)	
	Access Time	45nSec to 80nSec	10nSec to 15uSec (86)	
DRAM	Bits/Chip	16K	8K to 64K (86)	Only one military example in Data Base
	Refresh Rate	2K to 4KHz	2K to 4KHz (86)	
	Access Time	250nSec	80nSec to 460nSec (86)	
Misc.	No. of Stim. Inputs	12 to 128	22 to 118	
	No. of Resp. Outputs	16 to 128	15 to 229	
	No. of Bidirectional Lines	0 to 68	0 to 104	
	Stim. Voltage	-18V to +28V	-1.8V to +18V (86)	
	Resp. Voltage	-18V to +28V	-1.8V to +18V (86)	
	Sink Current	0 ma to 50** ma	0 to 50** ma (87)	**Estimated Worst Case

Table 1. Digital Data Technology Envelope (Cont'd)

Technology Area	Parameter	Range: Military Data Base	Range: Commercial Data Base	Notes
Misc. (Cont'd)	Source Current	0 ma to 50** ma	0 ma to 50** ma (87)	**Estimated worst case.
	Memory Storage (bytes)	0 to 8M	0 to 16M (87)	
	No. Logic Fam.	1 to 3	1 to 2 (87)	
	Clock Rate	256Hz to 9MHz	50KHz to 200MHz***	***Based on ATE survey interview data.
	Data Skew	30nSec to 1uSec	2nSec*** to 100nSec	
	Rise/Fall Time	10nSec to 200nSec	0.5nSec*** to 100nSec	
	No. of Required Power Supplies	1 to 5	1 to 4	
	Required Power Supplies Voltages	-30V to +30V	-12V to +12V	
	Serial Word Lengths	8 to 20 bits	8 bits	Only one commercial sample in Data Base
VHSIC Program	Component Dev Operating speed	25MHz to 80MHz (28, 37)	N/A	Two components developed; matrix switch, digital correlator.
MCF Program	CPU Clock Frequency	Technology Dependent (In order of 25 MHz)	N/A	No hardware developed. Preliminary specs for AN/UYK-41.
	Data Throughput	6 Mbytes/sec	N/A	
	CPU Word Length	32 bits	N/A	
	RAM Memory	4 to 8 Mbytes	N/A	
	EAROM Memory	128 to 512Kbytes	N/A	
	CPU Execution Rate	3 MIPS (goal)		

Because of the limited data rate and inflexible control scheme of the MIL-STD-1553 bus, there is currently under study a proposed High Speed Data Bus (HSDB) (27). This would differ from the MIL-STD-1553 bus in the following particulars:

- o distributed bus control
- o 20 Mbps data rate
- o audio signals integrated with data on the bus
- o bus size up to 64 terminals

Details concerning protocols have not yet been worked out for the HSDB.

The other busses listed in Table 2 are included either because they are used in the Army equipment included in the survey (RS-232 and current loop) or because they are equipment widely used in commercial. The IEEE-488 bus, which has been used in military ATE systems, is now finding application in commercial, non-ATE equipment and will probably be similarly employed in military equipment in the near future.

The serial busses listed in Table 2 require special interface hardware for testing, to generate the peculiar signal levels used. The parallel busses, however, use standard logic levels and interfacing test equipment. With parallel busses, it is simply a matter of generating and responding to handshaking control signals in accordance with the established bus protocols.

The lack of standardization in parallel data busses (other than IEEE-488) makes it difficult to project future developments in this area. However, some probable features of future parallel bus testing include:

- o higher data rates (100MHz or more)
- o lower signal levels
- o synchronous operation
- o impedance-matched RF transmission lines.

Figures 1 and 2 depict the current state of the art in semiconductor memories and microprocessors respectively, as well as the corresponding level of technology found in the Army equipment surveyed. It is apparent that the Army equipment is well behind the

Table 2. Data Busses

Bus Name	Type	Format	Data Rate
MIL-STD-1553	Serial	3 bit sync, 16 data bits, 1 parity bit	1 MHz
RS-232	Serial	2 data, 5 to 13 control lines, 8 bit word	20KHz
Current Loop	Serial	Start bit, 8 data bits, 1 or 2 stop bits	Asynch. (est. 9600 bps max.)
RS-449	Serial	2 data, 2 timing, 4 control lines, 8 bit words	Asynch. (10 M baud max.)
IEEE 488	Parallel	8 data, 3 control, 5 management	Asynch. (1 Mbytes/s max.)
DEC Unibus	Parallel	16 data, 18 address, 22 control	1.5MHz
Intel Multibus	Parallel	16 data, 16 address, 9 interrupts, 2 clocks, 11 controls	Asynch. (5 Mwords/sec. max.)

most advanced commercial devices. However, one of the goals of the VHSIC program is to reduce the gap between commercial and military technology, estimated at as much as 10 years or even longer (36). This reduction is to be achieved by directly applying newly developed technology to operational military systems.

The impact of state-of-the-art digital technology on Army ATE test requirements will be discussed in the second part of this study, ATE Digital Test Requirements. Also, these ATE test requirements will be projected with the digital technology by analyzing the current trends in commercial and military electronics. The range of the parameters in the projected ATE requirements will encompass both present-day equipment which will still be in operation and the most advanced equipment expected to be encountered.

9.4 DEVELOPMENT OF DIGITAL ATE DESIGN REQUIREMENTS

The envelope of future digital test requirements will provide the basis for deriving the design requirements of digital ATE. However, other factors which must be considered include the following:

- o the effects of BIT in reducing the speed and memory depth requirements of ATE
- o the effects of equipment fault-tolerant design on ATE
- o the possible lag between commercial and military adoption of advanced technology
- o the effects of design for testability (DFT) on ATE.

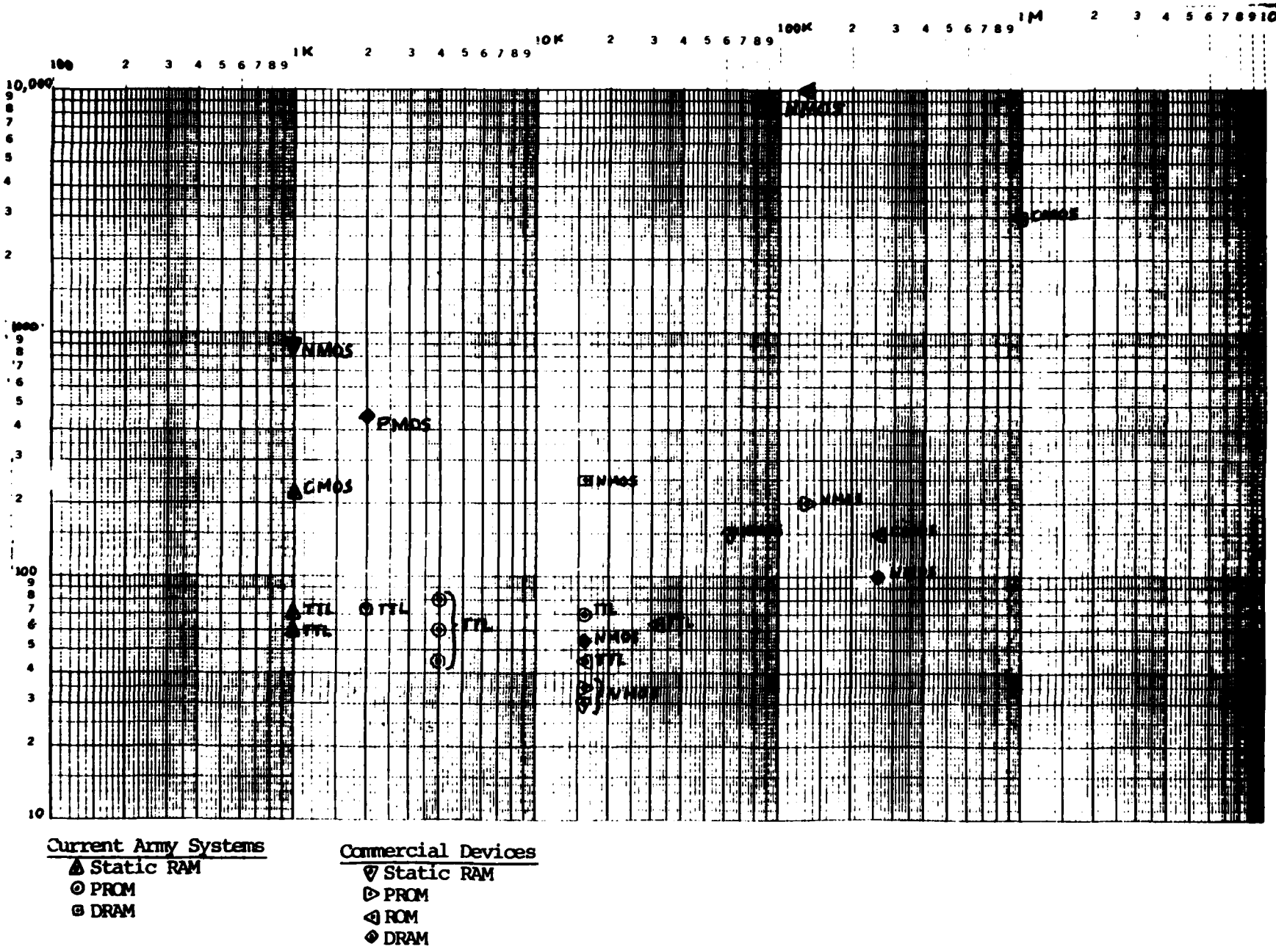


FIGURE 1. OVERVIEW of SPEED-DENSITY, SEMICONDUCTOR MEMORIES

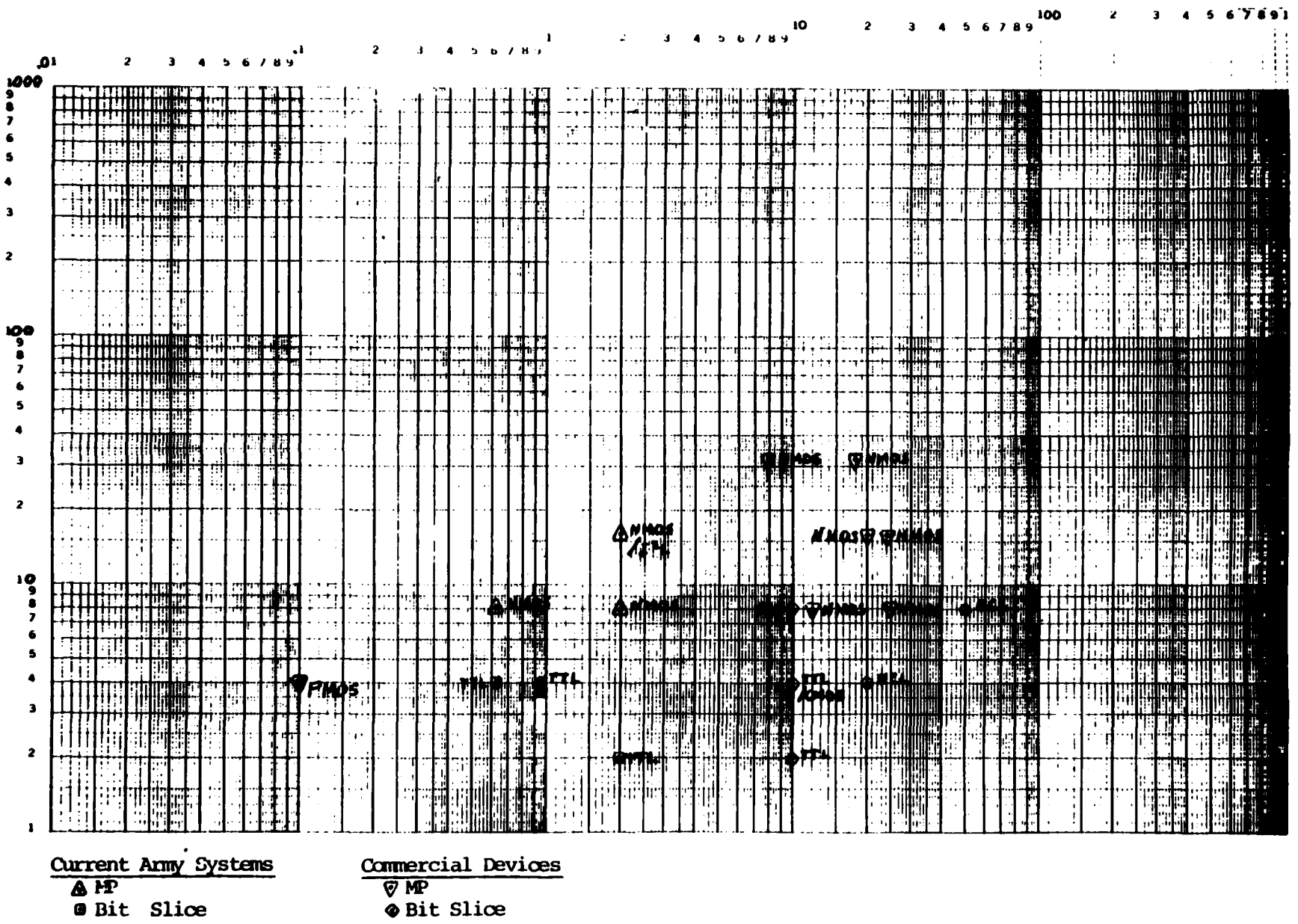


FIGURE 2. OVERVIEW of WORD LENGTH-CLOCK FREQENCY, MICROPROCESSORS

10.0 TEST REQUIREMENT PREMISES

10.1 DIGITAL TEST REQUIREMENT

Data has been obtained on present Army digital test requirements and future trends in digital circuit technology. These elements will be used to project a spectrum of future Army digital test requirements.

The premises used in analyzing the data to arrive at the projected digital test requirements are the following:

- o Dynamic Testing
  - — Dynamic LSI devices will require testing at operational frequencies in order to be tested functionally.
  - — Bi-directional busses will require tester driver/sensor pins to switch between inputs and outputs.
  - — The fault detection process will continue to become more and more complicated with the growth of microprocessor usage and complex bus structures in military systems. For this reason testers will be required to perform dynamic measurements in an accurate and timely fashion.
- o Digital Pattern Rate
  - — Dynamic testing will be required.
  - — Data rates will increase to over 100 MHz but will not be implemented in military fields systems in the 1988-1991 time frame.
  - — Clock rates will exceed 1.0 GHz but will not be implemented in military fields systems in the 1988-1991 time frame.
  - — Military adoption of advanced technology will continue to lag commercial.
- o Digital Stimulus Pattern Width
  - — The trend toward longer data words will continue beyond 32 bits, then level off.

- Systems will be more bus-oriented, reducing the number of random control and data signals required.

o Digital Measurement Pattern Width
(Same premises as Stimulus Pattern Width)

o Digital Pattern Depth

- Memory IC density will increase beyond 1 Mbit/chip.

o Maximum Allowable Skew Time

- Skew time must be less than the width of the system clock pulse.

o Internal or External Clock Synchronization

- Design-for-testability will make it possible for ATE to disable the internal system clock during testing.
- Design-for-testability rules will not always be followed.

o Programmable Strobe Delay

- Circuit propagation delays will continue to decrease, to well below 1nSec.
- Real-time dynamic testing will not be possible at the highest speeds expected.

o Programmable Stimulus Voltage Range and Accuracy

- Required voltages will not get any higher.
- They will be required to be set lower than at present.
- Lower levels will require finer resolution and accuracy.
- Today's higher levels will still be required.

- o Programmable Threshold Range and Accuracy
  (Same as Stimulus Voltage Range and Accuracy)

- o Maximum Source and Sink Current

  - — The requirements for source and sink currents are established by:
    logic levels
    circuit fan-in
    terminating resistors.
  - — Logic levels are going down.
  - — Bus-oriented systems typically have low fan-ins.
  - — Source and sink currents will be based on today's requirements, i.e., high-level signals and 50 to 130 ohm terminating resistors.

- o Maximum Digital Pulse Rate

  - — Maximum UUT clock rates will be beyond the capability of ATE.
  - — ATE clock/data rates will be much higher than at present, but not as high as maximum UUT rates.
  - — Bursts of data, at system clock rate, longer than today's ATE can supply, will be required.

10.2 DIGITAL ATE SYSTEM REQUIREMENTS

The digital test requirements projection will be used to generate a set of requirements for future Army digital ATE. Consideration will be given to factors such as built-in test, design for testability and fault tolerant design which will also affect the design of digital ATE.

In transforming the anticipated digital test requirements into a set of ATE requirements, the analysis will be based upon the following premises.

- o Maximum Number of Digital Test Pins

  - — Data and address word lengths will continue to increase.
  - — More bi-directional I/O lines will be used, reducing the pin count.

- Military electronics will be more and more organized around serial and/or parallel data busses rather than dedicated interfaces, also reducing pin count.

o Programmable Stimulus/Measurement/Tri-State

- Most, if not all, ATE digital test pins will be so programmable as to reduce the complexity of interface adapters.
- The use of bi-directional data busses will increase, strengthening the need for such programmability.

o Simultaneous Testing of Mixed Logic Families

- New, reduced power supply voltages and logic levels will be required to reduce power dissipation. These will be in addition to the present mix of logic levels.
- Military equipment will still require high-level signals, e.g., 28V relay closures and 12 to 15 volt high-noise-immunity logic.
- ATE will still have to handle older UUTs with a different mix of signal levels.

10.3 TEST PROGRAM SET DEVELOPMENT

The capabilities and limitations of today's manual and automated methods of TPS generation have been surveyed. Advanced methods of generating test program by means of computer-aided-design (CAD) and artificial intelligence (AI) are also under study. Recommendations for new or improved TPS generation tools will be provided.

The analysis and recommendations for improving the process of TPS development will be based on the following premises:

o Manual Generation

- Manual test pattern generation for VLSI devices will not be possible.
- Manual functional test generation, based on expected system performance, will still be possible in some cases.

- Capabilities of Available ATPGs

  - VLSI devices are already exceeding the capabilities of available ATPGs.
  - Gate level modelling of VLSI devices has about reached its limit.
  - Recent improvements to existing ATPGs, e.g., LASAR, show promise of increased ability to cope with VLSI.

- Recommendations for New/Enhanced ATPGs

  - Modelling at a higher level than the gate, e.g., the register, is required.
  - A higher level language is required.

- Other Means/Approaches of Digital TPS Generation

  - Increasingly, test pattern generation will be a by-product of CAD/CAM programs.
  - Heuristic (learning) programs will play an increasing part in automatic testing.

11.0 FOLLOW-ON REPORT

A follow-on report will describe the digital test requirements that resulted from the analysis and data collection performed for this report. This report is not intended to stand alone, but must be used in conjunction with the follow-on report which is entitled "Army Digital Test Requirements Report".

APPENDIX A

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APPENDIX B

Test Requirements Analysis (TRA)

MILITARY SYSTEM/BOARDS ELECTRONIC TEST EQUIPMENT PARAMETER REQUIREMENTS

System Nomenclature: CP-1406/TYQ
System/Board Contractor: N/S
Board Nomenclature: N/A
System/Board Source Document Number: TM11-5895-1020-14

	PARAMETER	UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
1.	Logic Family Types		TTL	1
2.	Maximum Data Rate	Mb/s	2	2
3.	Maximum Data Skew	nSEC	50 *	3
4.	Maximum No. of Stimulus Inputs		72	
5.	Maximum No. of Response Outputs		48	
6.	Programmable Stimulus Voltage Range	VOLTS	+0.0 to +5.0	
7.	Programmable Stimulus Voltage Resolution	VOLTS	0.1	
8.	Programmable Response Voltage Range	VOLTS	+0.0 to +5.0	
9.	Programmable Response Voltage Resolution	VOLTS	0.1	
10.	Logic "One" Voltage Maximum	VOLTS	+5.0	
11.	Logic "One" Voltage Minimum	VOLTS	+2.1	
12.	Logic "Zero" Voltage Maximum	VOLTS	+0.7	
13.	Logic "Zero" Voltage Minimum	VOLTS	+0.0	
14.	Maximum Rise Time	nSEC	200 *	
15.	Maximum Fall Time	nSEC	200 *	
16.	Maximum Input/Output Interface Sink Current	ma	50*	16
17.	Maximum Input/Output Interface Source Current	ma	50*	17
18.	Number of Power Supply Voltages Required		1	
19.	Power Supply Voltages	VOLTS	+5.0	
20.	Maximum Clock Rate	MHZ	2	20
21.	Serial Data Type		NRZ	21
22.	Maximum Serial Stimulus Word Length	BITS	8	
23.	Maximum Serial Response Word Length	BITS	8	
24.	No. of Bidirectional Lines		68	
25.	Total Used I/O PIN Count		120	
A.	Dynamic Testing		Yes	A
B.	Bidirectional Input/Output		Yes	B
C.	Bidirectional Bus		Yes	C
D.	Serial Node		Yes	D
E.	Pulse Catch		No	E
F.	Ready/Resume (Handshake)		Yes	F
G.	Architecture Function & Bus Type		RS232,20MA Loop	

PARAMETER		UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
H.	LSI & VLSI Types		UART, RAM	
I.	Microprocessor Type		9900	
J.	BIT Microprocessor Peripherals		N/A	
K.	Memory Type		RAM	
L.	Memory Size	BITS	32K x 32	

NOTES:

1. Use logic family names, such as TTL, ECL, CMOS, etc. for the logic the ATE must handle.
2. The maximum data rate in Mb/s that the ATE must supply.
3. The maximum deviation in time between data bits applied synchronously allowed for the ATE.
16. The maximum current ATE driver/receiver must handle to ground in milliamperes (ma).
17. The maximum current ATE driver/receiver must supply in milliamperes (ma).
20. The maximum clock frequency the ATE must supply.
21. The serial data type as RZ or NRZ the ATE must test.

A. A yes indicates that the ATE must test one or more signal properties or characteristics excluding voltage and current.

B,C,D. Enter yes if required.

E. A yes indicates that the ATE must detect and measure a oneshot output.

F. A yes indicates that the ATE must operate in a handshake mode of operation.

N/A Not applicable.

N/S Not specified.

* Estimated.

MILITARY SYSTEM/BOARDS ELECTRONIC TEST EQUIPMENT PARAMETER REQUIREMENTS

System Nomenclature: Patriot
System/Board Contractor: N/S
Board Nomenclature: N/A
System/Board Source Document Number: MIS-19975

	PARAMETER	UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
1.	Logic Family Types		TTL	1
2.	Maximum Data Rate	Mb/s	6	2
3.	Maximum Data Skew	nSEC	50 *	3
4.	Maximum No. of Stimulus Inputs		64	
5.	Maximum No. of Response Outputs		64	
6.	Programmable Stimulus Voltage Range	VOLTS	+0.0 to +5.0	
7.	Programmable Stimulus Voltage Resolution	VOLTS	0.1	
8.	Programmable Response Voltage Range	VOLTS	+0.0 to +5.0	
9.	Programmable Response Voltage Resolution	VOLTS	0.1	
10.	Logic "One" Voltage Maximum	VOLTS	+5.0	
11.	Logic "One" Voltage Minimum	VOLTS	+2.4	
12.	Logic "Zero" Voltage Maximum	VOLTS	+0.45	
13.	Logic "Zero" Voltage Minimum	VOLTS	+0.0	
14.	Maximum Rise Time	nSEC	10 *	
15.	Maximum Fall Time	nSEC	10 *	
16.	Maximum Input/Output Interface Sink Current	ma	50 *	16
17.	Maximum Input/Output Interface Source Current	ma	50 *	17
18.	Number of Power Supply Voltages Required		3	
19.	Power Supply Voltages	VOLTS	$\pm$ 5.0, + 12.0	
20.	Maximum Clock Rate	MHZ	6	20
21.	Serial Data Type		N/A	21
22.	Maximum Serial Stimulus Word Length	BITS	N/A	
23.	Maximum Serial Response Word Length	BITS	N/A	
24.	No. of Bidirectional Lines		None	
25.	Total Used I/O PIN Count		128	
A.	Dynamic Testing		Yes	A
B.	Bidirectional Input/Output		No	B
C.	Bidirectional Bus		No	C
D.	Serial Node		No	D
E.	Pulse Catch		No	E
F.	Ready/Resume (Handshake)		No	F
G.	Architecture Function & Bus Type		N/A	

PARAMETER		UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
H.	LSI & VLSI Types		DRAM, RAM	
I.	Microprocessor Type		N/A	
J.	BIT Microprocessor Peripherals		N/S	
K.	Memory Type		DRAM, RAM	
L.	Memory Size	BITS	16K x 15 & 1K x 25	

NOTES:

1. Use logic family names, such as TTL, ECL, CMOS, etc. for the logic the ATE must handle.
2. The maximum data rate in Mb/s that the ATE must supply.
3. The maximum deviation in time between data bits applied synchronously allowed for the ATE.
16. The maximum current ATE driver/receiver must handle to ground in milliamperes (ma).
17. The maximum current ATE driver/receiver must supply in milliamperes (ma).
20. The maximum clock frequency the ATE must supply.
21. The serial data type as RZ or NRZ the ATE must test.

A. A yes indicates that the ATE must test one or more signal properties or characteristics excluding voltage and current.

B,C,D. Enter yes if required.

E. A yes indicates that the ATE must detect and measure a oneshot output.

F. A yes indicates that the ATE must operate in a handshake mode of operation.

N/A Not applicable.

N/S Not specified.

* Estimated.

MILITARY SYSTEM/BOARDS ELECTRONIC TEST EQUIPMENT PARAMETER REQUIREMENTS

System Nomenclature: AN/PSG-2A
System/Board Contractor: N/S
Board Nomenclature: N/A
System/Board Source Document Number: TM-11-7440-281-30 & P

	PARAMETER	UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
1.	Logic Family Types		CMOS, TTL	1
2.	Maximum Data Rate	Mb/s	1	2
3.	Maximum Data Skew	nSEC	50 *	3
4.	Maximum No. of Stimulus Inputs		128	
5.	Maximum No. of Response Outputs		128	
6.	Programmable Stimulus Voltage Range	VOLTS	+0.0 to +12.0	
7.	Programmable Stimulus Voltage Resolution	VOLTS	0.05	
8.	Programmable Response Voltage Range	VOLTS	+0.0 to +12.0	
9.	Programmable Response Voltage Resolution	VOLTS	0.05	
10.	Logic "One" Voltage Maximum	VOLTS	+12.0, +5.0	
11.	Logic "One" Voltage Minimum	VOLTS	+11.95, +2.4	
12.	Logic "Zero" Voltage Maximum	VOLTS	+0.05, +0.5	
13.	Logic "Zero" Voltage Minimum	VOLTS	+0.0, +0.0	
14.	Maximum Rise Time	nSEC	50 *	
15.	Maximum Fall Time	nSEC	50 *	
16.	Maximum Input/Output Interface Sink Current	ma	50 *	16
17.	Maximum Input/Output Interface Source Current	ma	50 *	17
18.	Number of Power Supply Voltages Required		2	
19.	Power Supply Voltages	VOLTS	+5.0, +12.0	
20.	Maximum Clock Rate	MHZ	1	20
21.	Serial Data Type		NRZ	21
22.	Maximum Serial Stimulus Word Length	BITS	16	
23.	Maximum Serial Response Word Length	BITS	16	
24.	No. of Bidirectional Lines		N/S	
25.	Total Used I/O PIN Count		256	
A.	Dynamic Testing		Yes	A
B.	Bidirectional Input/Output		Yes	B
C.	Bidirectional Bus		Yes	C
D.	Serial Node		Yes	D
E.	Pulse Catch		No	E
F.	Ready/Resume (Handshake)		Yes	F
G.	Architecture Function & Bus Type		8 Bit (non-Std)	

PARAMETER		UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
H.	LSI & VLSI Types		RAM, PROM	
I.	Microprocessor Type		2901	
J.	BIT Microprocessor Peripherals		N/S	
K.	Memory Type		RAM, PROM	
L.	Memory Size	BITS	32K x 16	

NOTES:

1. Use logic family names, such as TTL, ECL, CMOS, etc. for the logic the ATE must handle.
2. The maximum data rate in Mb/s that the ATE must supply.
3. The maximum deviation in time between data bits applied synchronously allowed for the ATE.
16. The maximum current ATE driver/receiver must handle to ground in milliamperes (ma).
17. The maximum current ATE driver/receiver must supply in milliamperes (ma).
20. The maximum clock frequency the ATE must supply.
21. The serial data type as RZ or NRZ the ATE must test.

A. A yes indicates that the ATE must test one or more signal properties or characteristics excluding voltage and current.

B,C,D. Enter yes if required.

E. A yes indicates that the ATE must detect and measure a oneshot output.

F. A yes indicates that the ATE must operate in a handshake mode of operation.

N/A Not applicable.

N/S Not specified.

* Estimated.

MILITARY SYSTEM/BOARDS ELECTRONIC TEST EQUIPMENT PARAMETER REQUIREMENTS

System Nomenclature: MLRS
System/Board Contractor: Vought Corp.
Board Nomenclature: Volatile RAM
System/Board Source Document Number: Report No. 4.52300/1R-43

	PARAMETER	UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
1.	Logic Family Types		TTL	1
2.	Maximum Data Rate	Mb/s	N/S	2
3.	Maximum Data Skew	nSEC	100 *	3
4.	Maximum No. of Stimulus Inputs		36	
5.	Maximum No. of Response Outputs		24	
6.	Programmable Stimulus Voltage Range	VOLTS	+0.0 to +5.0	
7.	Programmable Stimulus Voltage Resolution	VOLTS	0.1	
8.	Programmable Response Voltage Range	VOLTS	+0.0 to +5.0	
9.	Programmable Response Voltage Resolution	VOLTS	0.1	
10.	Logic "One" Voltage Maximum	VOLTS	+5.0	
11.	Logic "One" Voltage Minimum	VOLTS	+2.4	
12.	Logic "Zero" Voltage Maximum	VOLTS	+0.5	
13.	Logic "Zero" Voltage Minimum	VOLTS	+0.0	
14.	Maximum Rise Time	nSEC	100 *	
15.	Maximum Fall Time	nSEC	100 *	
16.	Maximum Input/Output Interface Sink Current	ma	50 *	16
17.	Maximum Input/Output Interface Source Current	ma	50 *	17
18.	Number of Power Supply Voltages Required		3	
19.	Power Supply Voltages	VOLTS	+12.0, $\pm$5.0	
20.	Maximum Clock Rate	MHZ	N/S	20
21.	Serial Data Type		N/A	21
22.	Maximum Serial Stimulus Word Length	BITS	N/A	
23.	Maximum Serial Response Word Length	BITS	N/A	
24.	No. of Bidirectional Lines		None	
25.	Total Used I/O PIN Count		60	
A.	Dynamic Testing		No	A
B.	Bidirectional Input/Output		No	B
C.	Bidirectional Bus		No	C
D.	Serial Node		No	D
E.	Pulse Catch		No	E
F.	Ready/Resume (Handshake)		No	F
G.	Architecture Function & Bus Type		N/A	

PARAMETER		UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
H.	LSI & VLSI Types		RAM	
I.	Microprocessor Type		NONE	
J.	BIT Microprocessor Peripherals		NONE	
K.	Memory Type		RAM	
L.	Memory Size	BITS	16 K x 24	

NOTES:

1. Use logic family names, such as TTL, ECL, CMOS, etc. for the logic the ATE must handle.
2. The maximum data rate in Mb/s that the ATE must supply.
3. The maximum deviation in time between data bits applied synchronously allowed for the ATE.
16. The maximum current ATE driver/receiver must handle to ground in milliamperes (ma).
17. The maximum current ATE driver/receiver must supply in milliamperes (ma).
20. The maximum clock frequency the ATE must supply.
21. The serial data type as RZ or NRZ the ATE must test.

A. A yes indicates that the ATE must test one or more signal properties or characteristics excluding voltage and current.

B,C,D. Enter yes if required.

E. A yes indicates that the ATE must detect and measure a oneshot output.

F. A yes indicates that the ATE must operate in a handshake mode of operation.

N/A Not applicable.

N/S Not specified.

* Estimated.

MILITARY SYSTEM/BOARDS ELECTRONIC TEST EQUIPMENT PARAMETER REQUIREMENTS

System Nomenclature: MLRS
System/Board Contractor: Vought Corp.
Board Nomenclature: Memory Control
System/Board Source Document Number: DWG 1301380

	PARAMETER	UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
1.	Logic Family Types		TTL	1
2.	Maximum Data Rate	Mb/s	N/S	2
3.	Maximum Data Skew	nSEC	100 *	3
4.	Maximum No. of Stimulus Inputs		50	
5.	Maximum No. of Response Outputs		53	
6.	Programmable Stimulus Voltage Range	VOLTS	+0.0 to +5.0	
7.	Programmable Stimulus Voltage Resolution	VOLTS	0.1	
8.	Programmable Response Voltage Range	VOLTS	+0.0 to +5.0	
9.	Programmable Response Voltage Resolution	VOLTS	0.1	
10.	Logic "One" Voltage Maximum	VOLTS	+5.0	
11.	Logic "One" Voltage Minimum	VOLTS	+2.4	
12.	Logic "Zero" Voltage Maximum	VOLTS	+0.5	
13.	Logic "Zero" Voltage Minimum	VOLTS	+0.0	
14.	Maximum Rise Time	nSEC	100 *	
15.	Maximum Fall Time	nSEC	100 *	
16.	Maximum Input/Output Interface Sink Current	ma	50 *	16
17.	Maximum Input/Output Interface Source Current	ma	50 *	17
18.	Number of Power Supply Voltages Required		1	
19.	Power Supply Voltages	VOLTS	+5.0	
20.	Maximum Clock Rate	MHZ	N/S	20
21.	Serial Data Type		N/A	21
22.	Maximum Serial Stimulus Word Length	BITS	N/A	
23.	Maximum Serial Response Word Length	BITS	N/A	
24.	No. of Bidirectional Lines		18	
25.	Total Used I/O PIN Count		103	
A.	Dynamic Testing		No	A
B.	Bidirectional Input/Output		Yes	B
C.	Bidirectional Bus		Yes	C
D.	Serial Node		No	D
E.	Pulse Catch		No	E
F.	Ready/Resume (Handshake)		No	F
G.	Architecture Function & Bus Type		N/A	

PARAMETER		UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
H.	LSI & VLSI Types		PROM	
I.	Microprocessor Type		None	
J.	BIT Microprocessor Peripherals		None	
K.	Memory Type		PROM	
L.	Memory Size	BITS	1024 x 16	

NOTES:

1. Use logic family names, such as TTL, ECL, CMOS, etc. for the logic the ATE must handle.
2. The maximum data rate in Mb/s that the ATE must supply.
3. The maximum deviation in time between data bits applied synchronously allowed for the ATE.
16. The maximum current ATE driver/receiver must handle to ground in milliamperes (ma).
17. The maximum current ATE driver/receiver must supply in milliamperes (ma).
20. The maximum clock frequency the ATE must supply.
21. The serial data type as RZ or NRZ the ATE must test.

A. A yes indicates that the ATE must test one or more signal properties or characteristics excluding voltage and current.

B,C,D. Enter yes if required.

E. A yes indicates that the ATE must detect and measure a oneshot output.

F. A yes indicates that the ATE must operate in a handshake mode of operation.

N/A Not applicable.

N/S Not specified.

* Estimated.

MILITARY SYSTEM/BOARDS ELECTRONIC TEST EQUIPMENT PARAMETER REQUIREMENTS

System Nomenclature: MLRS
System/Board Contractor: Vought Corp.
Board Nomenclature: Fuze Setter
System/Board Source Document Number: Report No. 4-52300/IR-60

	PARAMETER	UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
1.	Logic Family Types		NMOS, TTL, CMOS	1
2.	Maximum Data Rate	Mb/s	6	2
3.	Maximum Data Skew	nSEC	50 *	3
4.	Maximum No. of Stimulus Inputs		27	
5.	Maximum No. of Response Outputs		16	
6.	Programmable Stimulus Voltage Range	VOLTS	+0.0 to +15.0	
7.	Programmable Stimulus Voltage Resolution	VOLTS	0.05	
8.	Programmable Response Voltage Range	VOLTS	+0.0 to +15.0	
9.	Programmable Response Voltage Resolution	VOLTS	0.05	
10.	Logic "One" Voltage Maximum	VOLTS	+5.0,+15.0	
11.	Logic "One" Voltage Minimum	VOLTS	+2.4,+14.95	
12.	Logic "Zero" Voltage Maximum	VOLTS	+0.8,+0.05	
13.	Logic "Zero" Voltage Minimum	VOLTS	+0.0,+0.0	
14.	Maximum Rise Time	nSEC	20 *	
15.	Maximum Fall Time	nSEC	20 *	
16.	Maximum Input/Output Interface Sink Current	ma	50 *	16
17.	Maximum Input/Output Interface Source Current	ma	50 *	17
18.	Number of Power Supply Voltages Required		5	
19.	Power Supply Voltages	VOLTS	+5.0, $\pm$15.0, $\pm$30.0	
20.	Maximum Clock Rate	MHZ	6.55	20
21.	Serial Data Type		N/A	21
22.	Maximum Serial Stimulus Word Length	BITS	N/A	
23.	Maximum Serial Response Word Length	BITS	N/A	
24.	No. of Bidirectional Lines		None	
25.	Total Used I/O PIN Count		43	
A.	Dynamic Testing		Yes	A
B.	Bidirectional Input/Output		No	B
C.	Bidirectional Bus		No	C
D.	Serial Node		No	D
E.	Pulse Catch		No	E
F.	Ready/Resume (Handshake)		No	F
G.	Architecture Function & Bus Type		N/A	

PARAMETER		UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
H.	LSI & VLSI Types		None	
I.	Microprocessor Type		None	
J.	BIT Microprocessor Peripherals		None	
K.	Memory Type		None	
L.	Memory Size	BITS	None	

NOTES:

1. Use logic family names, such as TTL, ECL, CMOS, etc. for the logic the ATE must handle.
2. The maximum data rate in Mb/s that the ATE must supply.
3. The maximum deviation in time between data bits applied synchronously allowed for the ATE.
16. The maximum current ATE driver/receiver must handle to ground in milliamperes (ma).
17. The maximum current ATE driver/receiver must supply in milliamperes (ma).
20. The maximum clock frequency the ATE must supply.
21. The serial data type as RZ or NRZ the ATE must test.

A. A yes indicates that the ATE must test one or more signal properties or characteristics excluding voltage and current.

B,C,D. Enter yes if required,

E. A yes indicates that the ATE must detect and measure a oneshot output.

F. A yes indicates that the ATE must operate in a handshake mode of operation.

N/A Not applicable.

N/S Not specified.

* Estimated.

MILITARY SYSTEM/BOARDS ELECTRONIC TEST EQUIPMENT PARAMETER REQUIREMENTS

System Nomenclature: MLRS
System/Board Contractor: Vought Corp.
Board Nomenclature: Communications Controller
System/Board Source Document Number: Report No. 4 52300/2R-05
MIS-35041

	PARAMETER	UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
1.	Logic Family Types		HTL, TTL, CMOS	1
2.	Maximum Data Rate	Mb/s	2	2
3.	Maximum Data Skew	nSEC	50 *	3
4.	Maximum No. of Stimulus Inputs		60	
5.	Maximum No. of Response Outputs		54	
6.	Programmable Stimulus Voltage Range	VOLTS	-18.0 to +18.0	
7.	Programmable Stimulus Voltage Resolution	VOLTS	0.05	
8.	Programmable Response Voltage Range	VOLTS	-18.0 to +18.0	
9.	Programmable Response Voltage Resolution	VOLTS	0.05	
10.	Logic "One" Voltage Maximum	VOLTS	-3.0, +5.0, +12.0	
11.	Logic "One" Voltage Minimum	VOLTS	-18.0, +2.4, +11.95	
12.	Logic "Zero" Voltage Maximum	VOLTS	+18.0, +0.5, +0.05	
13.	Logic "Zero" Voltage Minimum	VOLTS	+3.0, +0.0, +0.0	
14.	Maximum Rise Time	nSEC	50 *	
15.	Maximum Fall Time	nSEC	50 *	
16.	Maximum Input/Output Interface Sink Current	ma	50 *	16
17.	Maximum Input/Output Interface Source Current	ma	50 *	17
18.	Number of Power Supply Voltages Required		3	
19.	Power Supply Voltages	VOLTS	+5.0, ±12.0	
20.	Maximum Clock Rate	MHZ	2	20
21.	Serial Data Type		NRZ	21
22.	Maximum Serial Stimulus Word Length	BITS	N/S	
23.	Maximum Serial Response Word Length	BITS	N/S	
24.	No. of Bidirectional Lines		36	
25.	Total Used I/O PIN Count		114	
A.	Dynamic Testing		No	A
B.	Bidirectional Input/Output		Yes	B
C.	Bidirectional Bus		No	C
D.	Serial Node		Yes	D
E.	Pulse Catch		No	E
F.	Ready/Resume (Handshake)		No	F
G.	Architecture Function & Bus Type		Z80	

PARAMETER		UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
H.	LSI & VLSI Types		RAM, PROM	
I.	Microprocessor Type		Z80	
J.	BIT Microprocessor Peripherals		N/A	
K.	Memory Type		RAM, PROM	
L.	Memory Size	BITS	16K x N/S	

NOTES:

1. Use logic family names, such as TTL, ECL, CMOS, etc. for the logic the ATE must handle.
2. The maximum data rate in Mb/s that the ATE must supply.
3. The maximum deviation in time between data bits applied synchronously allowed for the ATE.
16. The maximum current ATE driver/receiver must handle to ground in milliamperes (ma).
17. The maximum current ATE driver/receiver must supply in milliamperes (ma).
20. The maximum clock frequency the ATE must supply.
21. The serial data type as RZ or NRZ the ATE must test.

A. A yes indicates that the ATE must test one or more signal properties or characteristics excluding voltage and current.

B,C,D. Enter yes if required.

E. A yes indicates that the ATE must detect and measure a oneshot output.

F. A yes indicates that the ATE must operate in a handshake mode of operation.

N/A Not applicable.

N/S Not specified.

* Estimated.

MILITARY SYSTEM/BOARDS ELECTRONIC TEST EQUIPMENT PARAMETER REQUIREMENTS

System Nomenclature: MLRS
System/Board Contractor: Vought Corp.
Board Nomenclature: Controller & Memory Interface
System/Board Source Document Number: MIS-31760

	PARAMETER	UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
1.	Logic Family Types		TTL, CMOS	1
2.	Maximum Data Rate	Kb/s	614	2
3.	Maximum Data Skew	nSEC	80 *	3
4.	Maximum No. of Stimulus Inputs		35	
5.	Maximum No. of Response Outputs		62	
6.	Programmable Stimulus Voltage Range	VOLTS	+0.0 to +12.0	
7.	Programmable Stimulus Voltage Resolution	VOLTS	0.05	
8.	Programmable Response Voltage Range	VOLTS	+0.0 to +12.0	
9.	Programmable Response Voltage Resolution	VOLTS	0.05	
10.	Logic "One" Voltage Maximum	VOLTS	+5.0 , +12.0	
11.	Logic "One" Voltage Minimum	VOLTS	+3.0 , +11.95	
12.	Logic "Zero" Voltage Maximum	VOLTS	+0.4 , +0.05	
13.	Logic "Zero" Voltage Minimum	VOLTS	+0.0 , +0.0	
14.	Maximum Rise Time	nSEC	100 *	
15.	Maximum Fall Time	nSEC	100 *	
16.	Maximum Input/Output Interface Sink Current	ma	50 *	16
17.	Maximum Input/Output Interface Source Current	ma	50 *	17
18.	Number of Power Supply Voltages Required		4	
19.	Power Supply Voltages	VOLTS	± 15.0, +5.0, +12.0	
20.	Maximum Clock Rate	KHZ	614	20
21.	Serial Data Type		NRZ	21
22.	Maximum Serial Stimulus Word Length	BITS	16	
23.	Maximum Serial Response Word Length	BITS	16	
24.	No. of Bidirectional Lines		24	
25.	Total Used I/O PIN Count		97	
A.	Dynamic Testing		Yes	A
B.	Bidirectional Input/Output		Yes	B
C.	Bidirectional Bus		Yes	C
D.	Serial Node		Yes	D
E.	Pulse Catch		No	E
F.	Ready/Resume (Handshake)		Yes	F
G.	Architecture Function & Bus Type		9080A	

PARAMETER		UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
H.	LSI & VLSI Types		RAM, UART, PROM	
I.	Microprocessor Type		9080A	
J.	BIT Microprocessor Peripherals		None	
K.	Memory Type		RAM, PROM	
L.	Memory Size	BITS	512 x 8, 4K x 8	

NOTES:

1. Use logic family names, such as TTL, ECL, CMOS, etc. for the logic the ATE must handle.
2. The maximum data rate in Mb/s that the ATE must supply.
3. The maximum deviation in time between data bits applied synchronously allowed for the ATE.
16. The maximum current ATE driver/receiver must handle to ground in milliamperes (ma).
17. The maximum current ATE driver/receiver must supply in milliamperes (ma).
20. The maximum clock frequency the ATE must supply.
21. The serial data type as RZ or NRZ the ATE must test.

A. A yes indicates that the ATE must test one or more signal properties or characteristics excluding voltage and current.

B,C,D. Enter yes if required.

E. A yes indicates that the ATE must detect and measure a oneshot output.

F. A yes indicates that the ATE must operate in a handshake mode of operation.

N/A Not applicable.

N/S Not specified.

* Estimated.

MILITARY SYSTEM/BOARDS ELECTRONIC TEST EQUIPMENT PARAMETER REQUIREMENTS

System Nomenclature: MLRS
System/Board Contractor: Vought Corp.
Board Nomenclature: NON-VOLATILE RAM
System/Board Source Document Number: Report No. 4-52300/1R-62

	PARAMETER	UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
1.	Logic Family Types		TTL, CMOS	1
2.	Maximum Data Rate	Mb/s	1	2
3.	Maximum Data Skew	nSEC	50 *	3
4.	Maximum No. of Stimulus Inputs		125	
5.	Maximum No. of Response Outputs		109	
6.	Programmable Stimulus Voltage Range	VOLTS	+0.0 to +12.0	
7.	Programmable Stimulus Voltage Resolution	VOLTS	0.05	
8.	Programmable Response Voltage Range	VOLTS	+0.0 to +12.0	
9.	Programmable Response Voltage Resolution	VOLTS	0.05	
10.	Logic "One" Voltage Maximum	VOLTS	+5.0, +12.0	
11.	Logic "One" Voltage Minimum	VOLTS	+2.4, +11.95	
12.	Logic "Zero" Voltage Maximum	VOLTS	+0.8, +0.05	
13.	Logic "Zero" Voltage Minimum	VOLTS	+0.0, +0.0	
14.	Maximum Rise Time	nSEC	100 *	
15.	Maximum Fall Time	nSEC	100 *	
16.	Maximum Input/Output Interface Sink Current	ma	50 *	16
17.	Maximum Input/Output Interface Source Current	ma	50 *	17
18.	Number of Power Supply Voltages Required		2	
19.	Power Supply Voltages	VOLTS	+5.0, +12.0	
20.	Maximum Clock Rate	MHZ	1	20
21.	Serial Data Type		N/A	21
22.	Maximum Serial Stimulus Word Length	BITS	N/A	
23.	Maximum Serial Response Word Length	BITS	N/A	
24.	No. of Bidirectional Lines		None	
25.	Total Used I/O PIN Count		234	
A.	Dynamic Testing		No	A
B.	Bidirectional Input/Output		No	B
C.	Bidirectional Bus		No	C
D.	Serial Node		No	D
E.	Pulse Catch		No	E
F.	Ready/Resume (Handshake)		No	F
G.	Architecture Function & Bus Type		N/A	

PARAMETER		UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
H.	LSI & VLSI Types		RAM	
I.	Microprocessor Type		NONE	
J.	BIT Microprocessor Peripherals		NONE	
K.	Memory Type		RAM	
L.	Memory Size	BITS	16K x 24	

NOTES:

1. Use logic family names, such as TTL, ECL, CMOS, etc. for the logic the ATE must handle.
2. The maximum data rate in Mb/s that the ATE must supply.
3. The maximum deviation in time between data bits applied synchronously allowed for the ATE.
16. The maximum current ATE driver/receiver must handle to ground in milliamperes (ma).
17. The maximum current ATE driver/receiver must supply in milliamperes (ma).
20. The maximum clock frequency the ATE must supply.
21. The serial data type as RZ or NRZ the ATE must test.

A. A yes indicates that the ATE must test one or more signal properties or characteristics excluding voltage and current.

B,C,D. Enter yes if required.

E. A yes indicates that the ATE must detect and measure a oneshot output.

F. A yes indicates that the ATE must operate in a handshake mode of operation.

N/A Not applicable.

N/S Not specified.

* Estimated.

MILITARY SYSTEM/BOARDS ELECTRONIC TEST EQUIPMENT PARAMETER REQUIREMENTS

System Nomenclature: MLRS
System/Board Contractor: Vought Corp.
Board Nomenclature: CPU Interface
System/Board Source Document Number: Report No. 4-52300/IR-28

	PARAMETER	UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
1.	Logic Family Types		CMOS, TTL	1
2.	Maximum Data Rate	Mb/s	1	2
3.	Maximum Data Skew	nSEC	50*, 30*	3
4.	Maximum No. of Stimulus Inputs		69	
5.	Maximum No. of Response Outputs		101	
6.	Programmable Stimulus Voltage Range	VOLTS	+0.0 to +10.0	
7.	Programmable Stimulus Voltage Resolution	VOLTS	0.05	
8.	Programmable Response Voltage Range	VOLTS	+0.0 to +10.0	
9.	Programmable Response Voltage Resolution	VOLTS	0.05	
10.	Logic "One" Voltage Maximum	VOLTS	+10.0, +5.0	
11.	Logic "One" Voltage Minimum	VOLTS	+9.95, +2.4	
12.	Logic "Zero" Voltage Maximum	VOLTS	+0.05, +0.5	
13.	Logic "Zero" Voltage Minimum	VOLTS	+0.0, +0.0	
14.	Maximum Rise Time	nSEC	50 *	
15.	Maximum Fall Time	nSEC	50 *	
16.	Maximum Input/Output Interface Sink Current	ma	50 *	16
17.	Maximum Input/Output Interface Source Current	ma	50 *	17
18.	Number of Power Supply Voltages Required		2	
19.	Power Supply Voltages	VOLTS	+5.0, +10.0	
20.	Maximum Clock Rate	MHZ	1	20
21.	Serial Data Type		N/A	21
22.	Maximum Serial Stimulus Word Length	BITS	N/A	
23.	Maximum Serial Response Word Length	BITS	N/A	
24.	No. of Bidirectional Lines		None	
25.	Total Used I/O PIN Count		170	
A.	Dynamic Testing		Yes	A
B.	Bidirectional Input/Output		No	B
C.	Bidirectional Bus		N/A	C
D.	Serial Node		No	D
E.	Pulse Catch		No	E
F.	Ready/Resume (Handshake)		No	F
G.	Architecture Function & Bus Type		N/A	

PARAMETER		UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
H.	LSI & VLSI Types		PROM	
I.	Microprocessor Type		NONE	
J.	BIT Microprocessor Peripherals		NONE	
K.	Memory Type		PROM	
L.	Memory Size	BITS	96 x 8	

NOTES:

1. Use logic family names, such as TTL, ECL, CMOS, etc. for the logic the ATE must handle.
2. The maximum data rate in Mb/s that the ATE must supply.
3. The maximum deviation in time between data bits applied synchronously allowed for the ATE.
16. The maximum current ATE driver/receiver must handle to ground in milliamperes (ma).
17. The maximum current ATE driver/receiver must supply in milliamperes (ma).
20. The maximum clock frequency the ATE must supply.
21. The serial data type as RZ or NRZ the ATE must test.

A. A yes indicates that the ATE must test one or more signal properties or characteristics excluding voltage and current.

B,C,D. Enter yes if required.

E. A yes indicates that the ATE must detect and measure a oneshot output.

F. A yes indicates that the ATE must operate in a handshake mode of operation.

N/A Not applicable.

N/S Not specified.

* Estimated.

MILITARY SYSTEM/BOARDS ELECTRONIC TEST EQUIPMENT PARAMETER REQUIREMENTS

System Nomenclature: MLRS
System/Board Contractor: Vought Corp.
Board Nomenclature: Symbol Gen
System/Board Source Document Number: DWG 13031350

	PARAMETER	UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
1.	Logic Family Types		TTL	1
2.	Maximum Data Rate	Kb/s	468	2
3.	Maximum Data Skew	nSEC	80 *	3
4.	Maximum No. of Stimulus Inputs		30	
5.	Maximum No. of Response Outputs		32	
6.	Programmable Stimulus Voltage Range	VOLTS	+0.0 to +5.0	
7.	Programmable Stimulus Voltage Resolution	VOLTS	0.1	
8.	Programmable Response Voltage Range	VOLTS	+0.0 to +5.0	
9.	Programmable Response Voltage Resolution	VOLTS	0.1	
10.	Logic "One" Voltage Maximum	VOLTS	+5.0	
11.	Logic "One" Voltage Minimum	VOLTS	+2.4	
12.	Logic "Zero" Voltage Maximum	VOLTS	+0.5	
13.	Logic "Zero" Voltage Minimum	VOLTS	+0.0	
14.	Maximum Rise Time	nSEC	50 *	
15.	Maximum Fall Time	nSEC	50 *	
16.	Maximum Input/Output Interface Sink Current	ma	50 *	16
17.	Maximum Input/Output Interface Source Current	ma	50 *	17
18.	Number of Power Supply Voltages Required		3	
19.	Power Supply Voltages	VOLTS	+12.0, +10.0, +5.0	
20.	Maximum Clock Rate	KHZ	468	20
21.	Serial Data Type		N/A	21
22.	Maximum Serial Stimulus Word Length	BITS	N/A	
23.	Maximum Serial Response Word Length	BITS	N/A	
24.	No. of Bidirectional Lines		12	
25.	Total Used I/O PIN Count		62	
A.	Dynamic Testing		No	A
B.	Bidirectional Input/Output		Yes	B
C.	Bidirectional Bus		No	C
D.	Serial Node		No	D
E.	Pulse Catch		No	E
F.	Ready/Resume (Handshake)		NO	F
G.	Architecture Function & Bus Type		N/A	

PARAMETER		UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
H.	LSI & VLSI Types		RAM, PROM	
I.	Microprocessor Type		NONE	
J.	BIT Microprocessor Peripherals		NONE	
K.	Memory Type		RAM, PROM	
L.	Memory Size	BITS	1024 x 8, 256 x 8, 2048 x 12	

NOTES:

1. Use logic family names, such as TTL, ECL, CMOS, etc. for the logic the ATE must handle.
2. The maximum data rate in Mb/s that the ATE must supply.
3. The maximum deviation in time between data bits applied synchronously allowed for the ATE.
16. The maximum current ATE driver/receiver must handle to ground in milliamperes (ma).
17. The maximum current ATE driver/receiver must supply in milliamperes (ma).
20. The maximum clock frequency the ATE must supply.
21. The serial data type as RZ or NRZ the ATE must test.

A. A yes indicates that the ATE must test one or more signal properties or characteristics excluding voltage and current.

B,C,D. Enter yes if required.

E. A yes indicates that the ATE must detect and measure a oneshot output.

F. A yes indicates that the ATE must operate in a handshake mode of operation.

N/A Not applicable.

N/S Not specified.

* Estimated.

MILITARY SYSTEM/BOARDS ELECTRONIC TEST EQUIPMENT PARAMETER REQUIREMENTS

System Nomenclature: MLRS
System/Board Contractor: Vought Corp.
Board Nomenclature: ROM
System/Board Source Document Number: Report No. 4-52300/IR-34

	PARAMETER	UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
1.	Logic Family Types		TTL	1
2.	Maximum Data Rate	Mb/s	N/S	2
3.	Maximum Data Skew	nSEC	100 *	3
4.	Maximum No. of Stimulus Inputs		15	
5.	Maximum No. of Response Outputs		25	
6.	Programmable Stimulus Voltage Range	VOLTS	+0.0 to +5.0	
7.	Programmable Stimulus Voltage Resolution	VOLTS	0.1	
8.	Programmable Response Voltage Range	VOLTS	+0.0 to +5.0	
9.	Programmable Response Voltage Resolution	VOLTS	0.1	
10.	Logic "One" Voltage Maximum	VOLTS	+5.0	
11.	Logic "One" Voltage Minimum	VOLTS	+2.4	
12.	Logic "Zero" Voltage Maximum	VOLTS	+0.5	
13.	Logic "Zero" Voltage Minimum	VOLTS	+0.0	
14.	Maximum Rise Time	nSEC	100 *	
15.	Maximum Fall Time	nSEC	100 *	
16.	Maximum Input/Output Interface Sink Current	ma	50 *	16
17.	Maximum Input/Output Interface Source Current	ma	50 *	17
18.	Number of Power Supply Voltages Required		2	
19.	Power Supply Voltages	VOLTS	+12.0, +5.0	
20.	Maximum Clock Rate	MHZ	N/A	20
21.	Serial Data Type		N/A	21
22.	Maximum Serial Stimulus Word Length	BITS	N/A	
23.	Maximum Serial Response Word Length	BITS	N/A	
24.	No. of Bidirectional Lines		None	
25.	Total Used I/O PIN Count		40	
A.	Dynamic Testing		No	A
B.	Bidirectional Input/Output		No	B
C.	Bidirectional Bus		No	C
D.	Serial Node		No	D
E.	Pulse Catch		No	E
F.	Ready/Resume (Handshake)		No	F
G.	Architecture Function & Bus Type		N/A	

PARAMETER		UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
H.	LSI & VLSI Types		PROM	
I.	Microprocessor Type		NONE	
J.	BIT Microprocessor Peripherals		NONE	
K.	Memory Type		PROM	
L.	Memory Size	BITS	24K x 24	

NOTES:

1. Use logic family names, such as TTL, ECL, CMOS, etc. for the logic the ATE must handle.
2. The maximum data rate in Mb/s that the ATE must supply.
3. The maximum deviation in time between data bits applied synchronously allowed for the ATE.
16. The maximum current ATE driver/receiver must handle to ground in milliamperes (ma).
17. The maximum current ATE driver/receiver must supply in milliamperes (ma).
20. The maximum clock frequency the ATE must supply.
21. The serial data type as RZ or NRZ the ATE must test.

A. A yes indicates that the ATE must test one or more signal properties or characteristics excluding voltage and current.

B,C,D. Enter yes if required.

E. A yes indicates that the ATE must detect and measure a oneshot output.

F. A yes indicates that the ATE must operate in a handshake mode of operation.

N/A Not applicable.

N/S Not specified.

* Estimated.

MILITARY SYSTEM/BOARDS ELECTRONIC TEST EQUIPMENT PARAMETER REQUIREMENTS

System Nomenclature: MLRS
System/Board Contractor: Vought Corp.
Board Nomenclature: Central Processor Unit
System/Board Source Document Number: Report No. 4-52300/IR-27A

	PARAMETER	UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
1.	Logic Family Types		TTL	1
2.	Maximum Data Rate	Kb/s	614	2
3.	Maximum Data Skew	nSEC	80 *	3
4.	Maximum No. of Stimulus Inputs		84	
5.	Maximum No. of Response Outputs		80	
6.	Programmable Stimulus Voltage Range	VOLTS	+0.0 to +5.0	
7.	Programmable Stimulus Voltage Resolution	VOLTS	0.1	
8.	Programmable Response Voltage Range	VOLTS	+0.0 to +5.0	
9.	Programmable Response Voltage Resolution	VOLTS	0.1	
10.	Logic "One" Voltage Maximum	VOLTS	+5.0	
11.	Logic "One" Voltage Minimum	VOLTS	+2.4	
12.	Logic "Zero" Voltage Maximum	VOLTS	+0.8	
13.	Logic "Zero" Voltage Minimum	VOLTS	+0.0	
14.	Maximum Rise Time	nSEC	50 *	
15.	Maximum Fall Time	nSEC	50 *	
16.	Maximum Input/Output Interface Sink Current	ma	50 *	16
17.	Maximum Input/Output Interface Source Current	ma	50 *	17
18.	Number of Power Supply Voltages Required		1	
19.	Power Supply Voltages	VOLTS	+5.0	
20.	Maximum Clock Rate	KHZ	614	20
21.	Serial Data Type		N/A	21
22.	Maximum Serial Stimulus Word Length	BITS	N/A	
23.	Maximum Serial Response Word Length	BITS	N/A	
24.	No. of Bidirectional Lines		26	
25.	Total Used I/O PIN Count		164	
A.	Dynamic Testing		Yes	A
B.	Bidirectional Input/Output		Yes	B
C.	Bidirectional Bus		Yes	C
D.	Serial Node		No	D
E.	Pulse Catch		No	E
F.	Ready/Resume (Handshake)		Yes	F
G.	Architecture Function & Bus Type		18 BIT Non-std	

PARAMETER		UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
H.	LSI & VLSI Types		RAM, PROM	
I.	Microprocessor Type		2901	
J.	BIT Microprocessor Peripherals		PROM	
K.	Memory Type		PROM	
L.	Memory Size	BITS	6K x 8, 512 x 16, 512 x 19	

NOTES:

1. Use logic family names, such as TTL, ECL, CMOS, etc. for the logic the ATE must handle.
2. The maximum data rate in Mb/s that the ATE must supply.
3. The maximum deviation in time between data bits applied synchronously allowed for the ATE.
16. The maximum current ATE driver/receiver must handle to ground in milliamperes (ma).
17. The maximum current ATE driver/receiver must supply in milliamperes (ma).
20. The maximum clock frequency the ATE must supply.
21. The serial data type as RZ or NRZ the ATE must test.

A. A yes indicates that the ATE must test one or more signal properties or characteristics excluding voltage and current.

B,C,D. Enter yes if required.

E. A yes indicates that the ATE must detect and measure a oneshot output.

F. A yes indicates that the ATE must operate in a handshake mode of operation.

N/A Not applicable.

N/S Not specified.

* Estimated.

MILITARY SYSTEM/BOARDS ELECTRONIC TEST EQUIPMENT PARAMETER REQUIREMENTS

System Nomenclature: Multiplexer TD-1236
System/Board Contractor: Raytheon
Board Nomenclature: Group Multiplexer/Demultiplexer
System/Board Source Document Number: DTM11-5805-697-34 & P

	PARAMETER	UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
1.	Logic Family Types		TTL	1
2.	Maximum Data Rate	Mb/s	4	2
3.	Maximum Data Skew	nSEC	40 *	3
4.	Maximum No. of Stimulus Inputs		49	
5.	Maximum No. of Response Outputs		38	
6.	Programmable Stimulus Voltage Range	VOLTS	+0.0 to +5.0	
7.	Programmable Stimulus Voltage Resolution	VOLTS	0.1	
8.	Programmable Response Voltage Range	VOLTS	+0.0 to +5.0	
9.	Programmable Response Voltage Resolution	VOLTS	0.1	
10.	Logic "One" Voltage Maximum	VOLTS	+5.0	
11.	Logic "One" Voltage Minimum	VOLTS	+2.0	
12.	Logic "Zero" Voltage Maximum	VOLTS	+0.5	
13.	Logic "Zero" Voltage Minimum	VOLTS	+0.0	
14.	Maximum Rise Time	nSEC	30 *	
15.	Maximum Fall Time	nSEC	30 *	
16.	Maximum Input/Output Interface Sink Current	ma	50 *	16
17.	Maximum Input/Output Interface Source Current	ma	50 *	17
18.	Number of Power Supply Voltages Required		1	
19.	Power Supply Voltages	VOLTS	+5.0	
20.	Maximum Clock Rate	MHZ	4	20
21.	Serial Data Type		NRZ	21
22.	Maximum Serial Stimulus Word Length	BITS	N/S	
23.	Maximum Serial Response Word Length	BITS	N/S	
24.	No. of Bidirectional Lines		NONE	
25.	Total Used I/O PIN Count		87	
A.	Dynamic Testing		Yes	A
B.	Bidirectional Input/Output		No	B
C.	Bidirectional Bus		NA	C
D.	Serial Node		Yes	D
E.	Pulse Catch		No	E
F.	Ready/Resume (Handshake)		Yes	F
G.	Architecture Function & Bus Type		N/A	

PARAMETER		UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
H.	LSI & VLSI Types		RAM, FIFO, Comparators	
I.	Microprocessor Type		N/A	
J.	BIT Microprocessor Peripherals		N/A	
K.	Memory Type		RAM	
L.	Memory Size	BITS	1K x 1	

NOTES:

1. Use logic family names, such as TTL, ECL, CMOS, etc. for the logic the ATE must handle.
2. The maximum data rate in Mb/s that the ATE must supply.
3. The maximum deviation in time between data bits applied synchronously allowed for the ATE.
16. The maximum current ATE driver/receiver must handle to ground in milliamperes (ma).
17. The maximum current ATE driver/receiver must supply in milliamperes (ma).
20. The maximum clock frequency the ATE must supply.
21. The serial data type as RZ or NRZ the ATE must test.

A. A yes indicates that the ATE must test one or more signal properties or characteristics excluding voltage and current.

B,C,D. Enter yes if required.

E. A yes indicates that the ATE must detect and measure a oneshot output.

F. A yes indicates that the ATE must operate in a handshake mode of operation.

N/A Not applicable.

N/S Not specified.

* Estimated.

MILITARY SYSTEM/BOARDS ELECTRONIC TEST EQUIPMENT PARAMETER REQUIREMENTS

System Nomenclature: Multiplexer TD-1236
System/Board Contractor: Raytheon
Board Nomenclature: Timing CCA
System/Board Source Document Number: CIM11-5805-697-34 & P

	PARAMETER	UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
1.	Logic Family Types		TTL	1
2.	Maximum Data Rate	Mb/s	4	2
3.	Maximum Data Skew	nSEC	50 *	3
4.	Maximum No. of Stimulus Inputs		25	
5.	Maximum No. of Response Outputs		48	
6.	Programmable Stimulus Voltage Range	VOLTS	+0.0 to +5.0	
7.	Programmable Stimulus Voltage Resolution	VOLTS	0.1	
8.	Programmable Response Voltage Range	VOLTS	+0.0 to +5.0	
9.	Programmable Response Voltage Resolution	VOLTS	0.1	
10.	Logic "One" Voltage Maximum	VOLTS	+5.0	
11.	Logic "One" Voltage Minimum	VOLTS	+2.0	
12.	Logic "Zero" Voltage Maximum	VOLTS	+0.5	
13.	Logic "Zero" Voltage Minimum	VOLTS	+0.0	
14.	Maximum Rise Time	nSEC	30 *	
15.	Maximum Fall Time	nSEC	30 *	
16.	Maximum Input/Output Interface Sink Current	ma	50 *	16
17.	Maximum Input/Output Interface Source Current	ma	50 *	17
18.	Number of Power Supply Voltages Required		1	
19.	Power Supply Voltages	VOLTS	+5.0	
20.	Maximum Clock Rate	MHZ	9	20
21.	Serial Data Type		NRZ	21
22.	Maximum Serial Stimulus Word Length	BITS	N/S	
23.	Maximum Serial Response Word Length	BITS	N/S	
24.	No. of Bidirectional Lines		NONE	
25.	Total Used I/O PIN Count		73	
A.	Dynamic Testing		Yes	A
B.	Bidirectional Input/Output		No	B
C.	Bidirectional Bus		No	C
D.	Serial Node		Yes	D
E.	Pulse Catch		No	E
F.	Ready/Resume (Handshake)		Yes	F
G.	Architecture Function & Bus Type		N/A	

PARAMETER		UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
H.	LSI & VLSI Types		Comparator, PROM	
I.	Microprocessor Type		N/A	
J.	BIT Microprocessor Peripherals		N/A	
K.	Memory Type		PROM	
L.	Memory Size	BITS	N/S	

NOTES:

1. Use logic family names, such as TTL, ECL, CMOS, etc. for the logic the ATE must handle.
2. *The maximum data rate in Mb/s that the ATE must supply.*
3. The maximum deviation in time between data bits applied synchronously allowed for the ATE.

16. The maximum current ATE driver/receiver must handle to ground in milliamperes (ma).
17. The maximum current ATE driver/receiver must supply in milliamperes (ma).
20. The maximum clock frequency the ATE must supply.
21. The serial data type as RZ or NRZ the ATE must test.

A. A yes indicates that the ATE must test one or more signal properties or characteristics excluding voltage and current.

B,C,D. Enter yes if required.

E. A yes indicates that the ATE must detect and measure a oneshot output.

F. A yes indicates that the ATE must operate in a handshake mode of operation.

N/A Not applicable.

N/S *Not specified.*

* Estimated.

MILITARY SYSTEM/BOARDS ELECTRONIC TEST EQUIPMENT PARAMETER REQUIREMENTS

System Nomenclature: Multiplexer TD-1236
System/Board Contractor: Raytheon
Board Nomenclature: BITE CCA
System/Board Source Document Number: DTM11-5805-697-34 & P

	PARAMETER	UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
1.	Logic Family Types		TTL	1
2.	Maximum Data Rate	b/s	256	2
3.	Maximum Data Skew	nSEC	100 *	3
4.	Maximum No. of Stimulus Inputs		25	
5.	Maximum No. of Response Outputs		75	
6.	Programmable Stimulus Voltage Range	VOLTS	+0.0 to +5.0	
7.	Programmable Stimulus Voltage Resolution	VOLTS	0.1	
8.	Programmable Response Voltage Range	VOLTS	+0.0 to +5.0	
9.	Programmable Response Voltage Resolution	VOLTS	0.1	
10.	Logic "One" Voltage Maximum	VOLTS	+5.0	
11.	Logic "One" Voltage Minimum	VOLTS	+2.0	
12.	Logic "Zero" Voltage Maximum	VOLTS	+0.5	
13.	Logic "Zero" Voltage Minimum	VOLTS	+0.0	
14.	Maximum Rise Time	nSEC	100 *	
15.	Maximum Fall Time	nSEC	100 *	
16.	Maximum Input/Output Interface Sink Current	ma	50 *	16
17.	Maximum Input/Output Interface Source Current	ma	50 *	17
18.	Number of Power Supply Voltages Required		2	
19.	Power Supply Voltages	VOLTS	+12, +5.0	
20.	Maximum Clock Rate	HZ	256	20
21.	Serial Data Type		N/A	21
22.	Maximum Serial Stimulus Word Length	BITS	N/A	
23.	Maximum Serial Response Word Length	BITS	N/A	
24.	No. of Bidirectional Lines		NONE	
25.	Total Used I/O PIN Count		100	
A.	Dynamic Testing		Yes	A
B.	Bidirectional Input/Output		No	B
C.	Bidirectional Bus		No	C
D.	Serial Node		No	D
E.	Pulse Catch		No	E
F.	Ready/Resume (Handshake)		Yes	F
G.	Architecture Function & Bus Type		N/A	

PARAMETER		UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
H.	LSI & VLSI Types		PROM	
I.	Microprocessor Type		N/A	
J.	BIT Microprocessor Peripherals		Yes (storage)	
K.	Memory Type		PROM	
L.	Memory Size	BITS	512 x 8	

NOTES:

1. Use logic family names, such as TTL, ECL, CMOS, etc. for the logic the ATE must handle.
2. The maximum data rate in Mb/s that the ATE must supply.
3. The maximum deviation in time between data bits applied synchronously allowed for the ATE.
16. The maximum current ATE driver/receiver must handle to ground in milliamperes (ma).
17. The maximum current ATE driver/receiver must supply in milliamperes (ma).
20. The maximum clock frequency the ATE must supply.
21. The serial data type as RZ or NRZ the ATE must test.

A. A yes indicates that the ATE must test one or more signal properties or characteristics excluding voltage and current.

B,C,D. Enter yes if required.

E. A yes indicates that the ATE must detect and measure a oneshot output.

F. A yes indicates that the ATE must operate in a handshake mode of operation.

N/A Not applicable.

N/S Not specified.

* Estimated.

MILITARY SYSTEM/BOARDS ELECTRONIC TEST EQUIPMENT PARAMETER REQUIREMENTS

System Nomenclature: Multiplexer TD-1236
System/Board Contractor: Raytheon
Board Nomenclature: Microcontroller
System/Board Source Document Number: DTM11-5805-697-34 & P

	PARAMETER	UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
1.	Logic Family Types		TTL	1
2.	Maximum Data Rate	Mb/s	2	2
3.	Maximum Data Skew	nSEC	50 *	3
4.	Maximum No. of Stimulus Inputs		46	
5.	Maximum No. of Response Outputs		43	
6.	Programmable Stimulus Voltage Range	VOLTS	+0.0 to +5.0	
7.	Programmable Stimulus Voltage Resolution	VOLTS	0.1	
8.	Programmable Response Voltage Range	VOLTS	+0.0 to +5.0	
9.	Programmable Response Voltage Resolution	VOLTS	0.1	
10.	Logic "One" Voltage Maximum	VOLTS	+5.0	
11.	Logic "One" Voltage Minimum	VOLTS	+2.0	
12.	Logic "Zero" Voltage Maximum	VOLTS	+0.5	
13.	Logic "Zero" Voltage Minimum	VOLTS	+0.0	
14.	Maximum Rise Time	nSEC	30 *	
15.	Maximum Fall Time	nSEC	30 *	
16.	Maximum Input/Output Interface Sink Current	ma	50 *	16
17.	Maximum Input/Output Interface Source Current	ma	50 *	17
18.	Number of Power Supply Voltages Required		1	
19.	Power Supply Voltages	VOLTS	+5.0	
20.	Maximum Clock Rate	MHZ	2	20
21.	Serial Data Type		NRZ	21
22.	Maximum Serial Stimulus Word Length	BITS	N/S	
23.	Maximum Serial Response Word Length	BITS	N/S	
24.	No. of Bidirectional Lines		None	
25.	Total Used I/O PIN Count		89	
A.	Dynamic Testing		Yes	A
B.	Bidirectional Input/Output		No	B
C.	Bidirectional Bus		No	C
D.	Serial Node		Yes	D
E.	Pulse Catch		No	E
F.	Ready/Resume (Handshake)		No	F
G.	Architecture Function & Bus Type		8 BIT	

PARAMETER		UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
H.	LSI & VLSI Types		PROM, RAM, Registers, Decoders	
I.	Microprocessor Type		2-BIT Slice	
J.	BIT Microprocessor Peripherals		None	
K.	Memory Type		RAM, PROM	
L.	Memory Size	BITS	N/S	

NOTES:

1. Use logic family names, such as TTL, ECL, CMOS, etc. for the logic the ATE must handle.
2. The maximum data rate in Mb/s that the ATE must supply.
3. The maximum deviation in time between data bits applied synchronously allowed for the ATE.
16. The maximum current ATE driver/receiver must handle to ground in milliamperes (ma).
17. The maximum current ATE driver/receiver must supply in milliamperes (ma).
20. The maximum clock frequency the ATE must supply.
21. The serial data type as RZ or NRZ the ATE must test.

A. A yes indicates that the ATE must test one or more signal properties or characteristics excluding voltage and current.

B,C,D. Enter yes if required.

E. A yes indicates that the ATE must detect and measure a oneshot output.

F. A yes indicates that the ATE must operate in a handshake mode of operation.

N/A Not applicable.

N/S Not specified.

* Estimated.

MILITARY SYSTEM/BOARDS ELECTRONIC TEST EQUIPMENT PARAMETER REQUIREMENTS

System Nomenclature: Multiplexer TD-1236
System/Board Contractor: Raytheon
Board Nomenclature: Super Group
System/Board Source Document Number: DIMI-5805-697-34 & P

	PARAMETER	UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
1.	Logic Family Types		TTL	1
2.	Maximum Data Rate	Mb/s	2	2
3.	Maximum Data Skew	nSEC	50 *	3
4.	Maximum No. of Stimulus Inputs		42	
5.	Maximum No. of Response Outputs		70	
6.	Programmable Stimulus Voltage Range	VOLTS	+0.0 to +5.0	
7.	Programmable Stimulus Voltage Resolution	VOLTS	0.1	
8.	Programmable Response Voltage Range	VOLTS	+0.0 to +5.0	
9.	Programmable Response Voltage Resolution	VOLTS	0.1	
10.	Logic "One" Voltage Maximum	VOLTS	+5.0	
11.	Logic "One" Voltage Minimum	VOLTS	+2.0	
12.	Logic "Zero" Voltage Maximum	VOLTS	+0.5	
13.	Logic "Zero" Voltage Minimum	VOLTS	+0.0	
14.	Maximum Rise Time	nSEC	30 *	
15.	Maximum Fall Time	nSEC	30 *	
16.	Maximum Input/Output Interface Sink Current	ma	50 *	16
17.	Maximum Input/Output Interface Source Current	ma	50 *	17
18.	Number of Power Supply Voltages Required		2	
19.	Power Supply Voltages	VOLTS	± 5.0	
20.	Maximum Clock Rate	MHZ	2	20
21.	Serial Data Type		NRZ	21
22.	Maximum Serial Stimulus Word Length	BITS	N/S	
23.	Maximum Serial Response Word Length	BITS	N/S	
24.	No. of Bidirectional Lines		NONE	
25.	Total Used I/O PIN Count		112	
A.	Dynamic Testing		Yes	A
B.	Bidirectional Input/Output		No	B
C.	Bidirectional Bus		No	C
D.	Serial Node		Yes	D
E.	Pulse Catch		No	E
F.	Ready/Resume (Handshake)		Yes	F
G.	Architecture Function & Bus Type		N/A	

PARAMETER		UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
H.	LSI & VLSI Types		RAM, Comparator, PROM	
I.	Microprocessor Type		N/A	
J.	BIT Microprocessor Peripherals		Storage Registers	
K.	Memory Type		RAM, PROM	
L.	Memory Size	BITS	1K x 2	

NOTES:

1. Use logic family names, such as TTL, ECL, CMOS, etc. for the logic the ATE must handle.
2. The maximum data rate in Mb/s that the ATE must supply.
3. The maximum deviation in time between data bits applied synchronously allowed for the ATE.
16. The maximum current ATE driver/receiver must handle to ground in milliamperes (ma).
17. The maximum current ATE driver/receiver must supply in milliamperes (ma).
20. The maximum clock frequency the ATE must supply.
21. The serial data type as RZ or NRZ the ATE must test.

A. A yes indicates that the ATE must test one or more signal properties or characteristics excluding voltage and current.

B,C,D. Enter yes if required.

E. A yes indicates that the ATE must detect and measure a oneshot output.

F. A yes indicates that the ATE must operate in a handshake mode of operation.

N/A Not applicable.

N/S Not specified.

* Estimated.

MILITARY SYSTEM/BOARDS ELECTRONIC TEST EQUIPMENT PARAMETER REQUIREMENTS

System Nomenclature: AN/AYK-14 (V)
System/Board Contractor: N/S
Board Nomenclature: N/A
System/Board Source Document Number: AS-4197(AV)

PARAMETER		UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
1.	Logic Family Types		TTL, NTDS	1
2.	Maximum Data Rate	Mb/s	1	2
3.	Maximum Data Skew	nSEC	50 *	3
4.	Maximum No. of Stimulus Inputs		128	
5.	Maximum No. of Response Outputs		128	
6.	Programmable Stimulus Voltage Range	VOLTS	-15.0 to +5.0	
7.	Programmable Stimulus Voltage Resolution	VOLTS	0.1	
8.	Programmable Response Voltage Range	VOLTS	-15.0 to +5.0	
9.	Programmable Response Voltage Resolution	VOLTS	0.1	
10.	Logic "One" Voltage Maximum	VOLTS	+5.0, +0.0	
11.	Logic "One" Voltage Minimum	VOLTS	+2.4, -1.0	
12.	Logic "Zero" Voltage Maximum	VOLTS	+0.5, -14.0	
13.	Logic "Zero" Voltage Minimum	VOLTS	+0.0, -15.0	
14.	Maximum Rise Time	nSEC	50 *	
15.	Maximum Fall Time	nSEC	50 *	
16.	Maximum Input/Output Interface Sink Current	ma	50 *	16
17.	Maximum Input/Output Interface Source Current	ma	50 *	17
18.	Number of Power Supply Voltages Required		2	
19.	Power Supply Voltages	VOLTS	+5.0, -15.0	
20.	Maximum Clock Rate	MHZ	1.0	20
21.	Serial Data Type		NRZ	21
22.	Maximum Serial Stimulus Word Length	BITS	20	
23.	Maximum Serial Response Word Length	BITS	20	
24.	No. of Bidirectional Lines		16	
25.	Total Used I/O PIN Count		256	
A.	Dynamic Testing		Yes	A
B.	Bidirectional Input/Output		Yes	B
C.	Bidirectional Bus		Yes	C
D.	Serial Node		Yes	D
E.	Pulse Catch		No	E
F.	Ready/Resume (Handshake)		Yes	F
G.	Architecture Function & Bus Type		MIL-STD-1553, RS232	

PARAMETER		UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
H.	LSI & VLSI Types		N/A	
I.	Microprocessor Type		N/A	
J.	BIT Microprocessor Peripherals		Yes (N/S)	
K.	Memory Type		Core & Semicon	
L.	Memory Size	BITS	32K x 18 or 16K x 18	

NOTES:

1. Use logic family names, such as TTL, ECL, CMOS, etc. for the logic the ATE must handle.
2. The maximum data rate in Mb/s that the ATE must supply.
3. The maximum deviation in time between data bits applied synchronously allowed for the ATE.
16. The maximum current ATE driver/receiver must handle to ground in milliamperes (ma).
17. The maximum current ATE driver/receiver must supply in milliamperes (ma).
20. The maximum clock frequency the ATE must supply.
21. The serial data type as RZ or NRZ the ATE must test.

A. A yes indicates that the ATE must test one or more signal properties or characteristics excluding voltage and current.

B,C,D. Enter yes if required.

E. A yes indicates that the ATE must detect and measure a oneshot output.

F. A yes indicates that the ATE must operate in a handshake mode of operation.

N/A Not applicable.

N/S Not specified.

* Estimated.

MILITARY SYSTEM/BOARDS ELECTRONIC TEST EQUIPMENT PARAMETER REQUIREMENTS

System Nomenclature: XM-22
System/Board Contractor: N/S
Board Nomenclature: N/A
System/Board Source Document Number: TM 9-1270-218-13 & P

	PARAMETER	UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
1.	Logic Family Types		28V Discrete, TTL	1
2.	Maximum Data Rate	Mb/s	3.36	2
3.	Maximum Data Skew	nSEC	50 *	3
4.	Maximum No. of Stimulus Inputs		12	
5.	Maximum No. of Response Outputs		20	
6.	Programmable Stimulus Voltage Range	VOLTS	+0.0 to +28.0	
7.	Programmable Stimulus Voltage Resolution	VOLTS	0.1	
8.	Programmable Response Voltage Range	VOLTS	+0.0 to +28.0	
9.	Programmable Response Voltage Resolution	VOLTS	0.1	
10.	Logic "One" Voltage Maximum	VOLTS	+28.0, +5.0	
11.	Logic "One" Voltage Minimum	VOLTS	N/S, +2.4	
12.	Logic "Zero" Voltage Maximum	VOLTS	N/S, +0.5	
13.	Logic "Zero" Voltage Minimum	VOLTS	+0.0, +0.0	
14.	Maximum Rise Time	nSEC	20 *	
15.	Maximum Fall Time	nSEC	20 *	
16.	Maximum Input/Output Interface Sink Current	ma	50 *	16
17.	Maximum Input/Output Interface Source Current	ma	50 *	17
18.	Number of Power Supply Voltages Required		1	
19.	Power Supply Voltages	VOLTS	+28.0	
20.	Maximum Clock Rate	MHZ	3.36	20
21.	Serial Data Type		NRZ	21
22.	Maximum Serial Stimulus Word Length	BITS	11	
23.	Maximum Serial Response Word Length	BITS	11	
24.	No. of Bidirectional Lines		NONE	
25.	Total Used I/O PIN Count		32	
A.	Dynamic Testing		Yes	A
B.	Bidirectional Input/Output		No	B
C.	Bidirectional Bus		No	C
D.	Serial Node		Yes	D
E.	Pulse Catch		No	E
F.	Ready/Resume (Handshake)		Yes	F
G.	Architecture Function & Bus Type		I6 BIT (Non-Std)	

PARAMETER		UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
H.	LSI & VLSI Types		RAM, UART, PROM	
I.	Microprocessor Type		N/A	
J.	BIT Microprocessor Peripherals		D/A Sample & Hold	
K.	Memory Type		RAM, PROM	
L.	Memory Size	BITS	2K x 16, 8K x 16	

NOTES:

1. Use logic family names, such as TTL, ECL, CMOS, etc. for the logic the ATE must handle.
2. The maximum data rate in Mb/s that the ATE must supply.
3. The maximum deviation in time between data bits applied synchronously allowed for the ATE.
16. The maximum current ATE driver/receiver must handle to ground in milliamperes (ma).
17. The maximum current ATE driver/receiver must supply in milliamperes (ma).
20. The maximum clock frequency the ATE must supply.
21. The serial data type as RZ or NRZ the ATE must test.

A. A yes indicates that the ATE must test one or more signal properties or characteristics excluding voltage and current.

B,C,D. Enter yes if required.

E. A yes indicates that the ATE must detect and measure a oneshot output.

F. A yes indicates that the ATE must operate in a handshake mode of operation.

N/A Not applicable.

N/S Not specified.

* Estimated.

COMMERCIAL SYSTEM/BOARDS ELECTRONIC TEST EQUIPMENT PARAMETER REQUIREMENTS

System Nomenclature: iSBC 064
System/Board Contractor: Intel
Board Nomenclature: RAM, 64K Bytes
System/Board Source Document Number: Intel System Data Catalog

	PARAMETER	UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
1.	Logic Family Types		HMOS	1
2.	Maximum Data Rate	Kb/s Read 735nSec,Write 1360nSec		2
3.	Maximum Data Skew	nSEC	100 *	3
4.	Maximum No. of Stimulus Inputs		23	
5.	Maximum No. of Response Outputs		15	
6.	Programmable Stimulus Voltage Range	VOLTS	-0.5 to +5.0	
7.	Programmable Stimulus Voltage Resolution	VOLTS	0.1	
8.	Programmable Response Voltage Range	VOLTS	-0.5 to +5.0	
9.	Programmable Response Voltage Resolution	VOLTS	0.1	
10.	Logic "One" Voltage Maximum	VOLTS	+5.0	
11.	Logic "One" Voltage Minimum	VOLTS	+2.0	
12.	Logic "Zero" Voltage Maximum	VOLTS	+0.8	
13.	Logic "Zero" Voltage Minimum	VOLTS	-0.5	
14.	Maximum Rise Time	nSEC	50 *	
15.	Maximum Fall Time	nSEC	50 *	
16.	Maximum Input/Output Interface Sink Current	ma	50 *	16
17.	Maximum Input/Output Interface Source Current	ma	50 *	17
18.	Number of Power Supply Voltages Required		3	
19.	Power Supply Voltages	VOLTS	+12.0, $\pm$ 5.0	
20.	Maximum Clock Rate	KHZ	0.5	20
21.	Serial Data Type		N/A	21
22.	Maximum Serial Stimulus Word Length	BITS	N/A	
23.	Maximum Serial Response Word Length	BITS	N/A	
24.	No. of Bidirectional Lines		16	
25.	Total Used I/O PIN Count		38	
A.	Dynamic Testing		Yes	A
B.	Bidirectional Input/Output		Yes	B
C.	Bidirectional Bus		Yes	C
D.	Serial Node		No	D
E.	Pulse Catch		No	E
F.	Ready/Resume (Handshake)		Yes	F
G.	Architecture Function & Bus Type		Multibus	

PARAMETER		UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
H.	LSI & VLSI Types		DRAM	
I.	Microprocessor Type		None	
J.	BIT Microprocessor Peripherals		None	
K.	Memory Type		DRAM	
L.	Memory Size	BITS	64K x 8	

NOTES:

1. Use logic family names, such as TTL, ECL, CMOS, etc. for the logic the ATE must handle.
2. The maximum data rate in Mb/s that the ATE must supply.
3. The maximum deviation in time between data bits applied synchronously allowed for the ATE.
16. The maximum current ATE driver/receiver must handle to ground in milliamperes (ma).
17. The maximum current ATE driver/receiver must supply in milliamperes (ma).
20. The maximum clock frequency the ATE must supply.
21. The serial data type as RZ or NRZ the ATE must test.

A. A yes indicates that the ATE must test one or more signal properties or characteristics excluding voltage and current.

B,C,D. Enter yes if required.

E. A yes indicates that the ATE must detect and measure a oneshot output.

F. A yes indicates that the ATE must operate in a handshake mode of operation.

N/A Not applicable.

N/S Not specified.

* Estimated.

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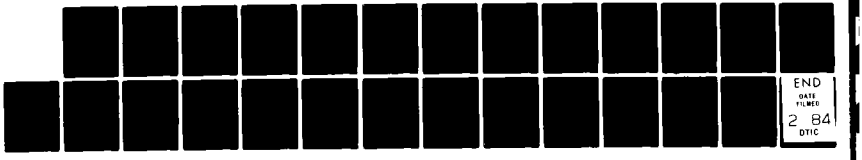
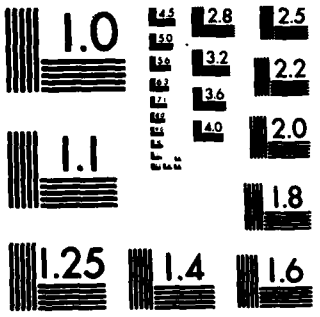




COMMERCIAL SYSTEM/BOARDS ELECTRONIC TEST EQUIPMENT PARAMETER REQUIREMENTS

System Nomenclature: iSBC 501
System/Board Contractor: Intel
Board Nomenclature: DMA Controller
System/Board Source Document Number: Intel System Data Catalog

PARAMETER		UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
1.	Logic Family Types		TTL	1
2.	Maximum Data Rate	Mb/s	1	2
3.	Maximum Data Skew	nSEC	50 *	3
4.	Maximum No. of Stimulus Inputs		34	
5.	Maximum No. of Response Outputs		28	
6.	Programmable Stimulus Voltage Range	VOLTS	+0.0 to +5.0	
7.	Programmable Stimulus Voltage Resolution	VOLTS	0.1	
8.	Programmable Response Voltage Range	VOLTS	+0.0 to +5.0	
9.	Programmable Response Voltage Resolution	VOLTS	0.1	
10.	Logic "One" Voltage Maximum	VOLTS	+5.0	
11.	Logic "One" Voltage Minimum	VOLTS	+2.0	
12.	Logic "Zero" Voltage Maximum	VOLTS	+0.8	
13.	Logic "Zero" Voltage Minimum	VOLTS	+0.0	
14.	Maximum Rise Time	nSEC	50 *	
15.	Maximum Fall Time	nSEC	50 *	
16.	Maximum Input/Output Interface Sink Current	ma	48	16
17.	Maximum Input/Output Interface Source Current	ma	48	17
18.	Number of Power Supply Voltages Required		1	
19.	Power Supply Voltages	VOLTS	+5.0	
20.	Maximum Clock Rate	MHZ	1	20
21.	Serial Data Type		N/A	21
22.	Maximum Serial Stimulus Word Length	BITS	N/A	
23.	Maximum Serial Response Word Length	BITS	N/A	
24.	No. of Bidirectional Lines		32	
25.	Total Used I/O PIN Count		62	
A.	Dynamic Testing		Yes	A
B.	Bidirectional Input/Output		Yes	B
C.	Bidirectional Bus		Yes	C
D.	Serial Node		No	D
E.	Pulse Catch		No	E
F.	Ready/Resume (Handshake)		Yes	F
G.	Architecture Function & Bus Type		Multibus	

PARAMETER		UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
H.	LSI & VLSI Types		Interrupt Control	
I.	Microprocessor Type		None	
J.	BIT Microprocessor Peripherals		None	
K.	Memory Type		None	
L.	Memory Size	BITS	None	

NOTES:

1. Use logic family names, such as TTL, ECL, CMOS, etc. for the logic the ATE must handle.
2. The maximum data rate in Mb/s that the ATE must supply.
3. The maximum deviation in time between data bits applied synchronously allowed for the ATE.
16. The maximum current ATE driver/receiver must handle to ground in milliamperes (ma).
17. The maximum current ATE driver/receiver must supply in milliamperes (ma).
20. The maximum clock frequency the ATE must supply.
21. The serial data type as RZ or NRZ the ATE must test.

A. A yes indicates that the ATE must test one or more signal properties or characteristics excluding voltage and current.

B,C,D. Enter yes if required.

E. A yes indicates that the ATE must detect and measure a oneshot output.

F. A yes indicates that the ATE must operate in a handshake mode of operation.

N/A Not applicable.

N/S Not specified.

* Estimated.

COMMERCIAL SYSTEM/BOARDS ELECTRONIC TEST EQUIPMENT PARAMETER REQUIREMENTS

System Nomenclature: iSBEC 544
System/Board Contractor: Intel
Board Nomenclature: Intelligent Communications Controller
System/Board Source Document Number: Intel System Data Catalog

	PARAMETER	UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
1.	Logic Family Types		NMOS	1
2.	Maximum Data Rate	Mb/s	1.22	2
3.	Maximum Data Skew	nSEC	50 *	3
4.	Maximum No. of Stimulus Inputs		31	
5.	Maximum No. of Response Outputs		22	
6.	Programmable Stimulus Voltage Range	VOLTS	-0.5 to +5.0	
7.	Programmable Stimulus Voltage Resolution	VOLTS	0.1	
8.	Programmable Response Voltage Range	VOLTS	-0.5 to +5.0	
9.	Programmable Response Voltage Resolution	VOLTS	0.1	
10.	Logic "One" Voltage Maximum	VOLTS	+5.0	
11.	Logic "One" Voltage Minimum	VOLTS	+2.0	
12.	Logic "Zero" Voltage Maximum	VOLTS	+0.8	
13.	Logic "Zero" Voltage Minimum	VOLTS	-0.5	
14.	Maximum Rise Time	nSEC	50 *	
15.	Maximum Fall Time	nSEC	50 *	
16.	Maximum Input/Output Interface Sink Current	ma	50 *	16
17.	Maximum Input/Output Interface Source Current	ma	50 *	17
18.	Number of Power Supply Voltages Required		4	
19.	Power Supply Voltages	VOLTS	$\pm$ 12.0, $\pm$ 5.0	
20.	Maximum Clock Rate	MHZ	1.2288	20
21.	Serial Data Type		NRZ	21
22.	Maximum Serial Stimulus Word Length	BITS	8	
23.	Maximum Serial Response Word Length	BITS	8	
24.	No. of Bidirectional Lines		40	
25.	Total Used I/O PIN Count		53	
A.	Dynamic Testing		Yes	A
B.	Bidirectional Input/Output		Yes	B
C.	Bidirectional Bus		Yes	C
D.	Serial Node		Yes	D
E.	Pulse Catch		No	E
F.	Ready/Resume (Handshake)		Yes	F
G.	Architecture Function & Bus Type		RS232C, Multibus	

PARAMETER		UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
H.	LSI & VLSI Types		ROM, DRAM, USART	
I.	Microprocessor Type		8085	
J.	BIT Microprocessor Peripherals		None	
K.	Memory Type		ROM, DRAM	
L.	Memory Size	BITS	8K x 8, 16K x 8	

NOTES:

1. Use logic family names, such as TTL, ECL, CMOS, etc. for the logic the ATE must handle.
2. The maximum data rate in Mb/s that the ATE must supply.
3. The maximum deviation in time between data bits applied synchronously allowed for the ATE.
16. The maximum current ATE driver/receiver must handle to ground in milliamperes (ma).
17. The maximum current ATE driver/receiver must supply in milliamperes (ma).
20. The maximum clock frequency the ATE must supply.
21. The serial data type as RZ or NRZ the ATE must test.

A. A yes indicates that the ATE must test one or more signal properties or characteristics excluding voltage and current.

B,C,D. Enter yes if required.

E. A yes indicates that the ATE must detect and measure a oneshot output.

F. A yes indicates that the ATE must operate in a handshake mode of operation.

N/A Not applicable.

N/S Not specified.

* Estimated.

COMMERCIAL SYSTEM/BOARDS ELECTRONIC TEST EQUIPMENT PARAMETER REQUIREMENTS

System Nomenclature: iSBC 86/12A
System/Board Contractor: Intel
Board Nomenclature: Single Board Computer
System/Board Source Document Number: Intel System Data Catalog

	PARAMETER	UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
1.	Logic Family Types		HMOS	1
2.	Maximum Data Rate	Mb/s	5.0	2
3.	Maximum Data Skew	nSEC	50 *	3
4.	Maximum No. of Stimulus Inputs		22	
5.	Maximum No. of Response Outputs		31	
6.	Programmable Stimulus Voltage Range	VOLTS	-0.5 to +5.0	
7.	Programmable Stimulus Voltage Resolution	VOLTS	0.1	
8.	Programmable Response Voltage Range	VOLTS	-0.5 to +5.0	
9.	Programmable Response Voltage Resolution	VOLTS	0.1	
10.	Logic "One" Voltage Maximum	VOLTS	+5.0	
11.	Logic "One" Voltage Minimum	VOLTS	+2.0	
12.	Logic "Zero" Voltage Maximum	VOLTS	+0.8	
13.	Logic "Zero" Voltage Minimum	VOLTS	-0.5	
14.	Maximum Rise Time	nSEC	20 *	
15.	Maximum Fall Time	nSEC	20 *	
16.	Maximum Input/Output Interface Sink Current	ma	50 *	16
17.	Maximum Input/Output Interface Source Current	ma	50 *	17
18.	Number of Power Supply Voltages Required		4	
19.	Power Supply Voltages	VOLTS	±12.0, ±5.0	
20.	Maximum Clock Rate	MHZ	5.0	20
21.	Serial Data Type		NRZ	21
22.	Maximum Serial Stimulus Word Length	BITS	8	
23.	Maximum Serial Response Word Length	BITS	8	
24.	No. of Bidirectional Lines		40	
25.	Total Used I/O PIN Count		53	
A.	Dynamic Testing		Yes	A
B.	Bidirectional Input/Output		Yes	B
C.	Bidirectional Bus		Yes	C
D.	Serial Node		Yes	D
E.	Pulse Catch		No	E
F.	Ready/Resume (Handshake)		Yes	F
G.	Architecture Function & Bus Type		RS232C, Multibus	

PARAMETER		UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
H.	LSI & VLSI Types		ROM, RAM, USART	
I.	Microprocessor Type		8086	
J.	BIT Microprocessor Peripherals		None	
K.	Memory Type		ROM, RAM	
L.	Memory Size	BITS	16K x 8, 32K x 8	

NOTES:

1. Use logic family names, such as TTL, ECL, CMOS, etc. for the logic the ATE must handle.
2. The maximum data rate in Mb/s that the ATE must supply.
3. The maximum deviation in time between data bits applied synchronously allowed for the ATE.
16. The maximum current ATE driver/receiver must handle to ground in milliamperes (ma).
17. The maximum current ATE driver/receiver must supply in milliamperes (ma).
20. The maximum clock frequency the ATE must supply.
21. The serial data type as RZ or NRZ the ATE must test.

A. A yes indicates that the ATE must test one or more signal properties or characteristics excluding voltage and current.

B,C,D. Enter yes if required.

E. A yes indicates that the ATE must detect and measure a oneshot output.

F. A yes indicates that the ATE must operate in a handshake mode of operation.

N/A Not applicable.

N/S Not specified.

* Estimated.

COMMERCIAL SYSTEM/BOARDS ELECTRONIC TEST EQUIPMENT PARAMETER REQUIREMENTS

System Nomenclature: iSBC 254
System/Board Contractor: Intel
Board Nomenclature: Bubble Memory
System/Board Source Document Number: Intel System Data Catalog

	PARAMETER	UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
1.	Logic Family Types		TTL, Bubble	1
2.	Maximum Data Rate	Kb/s	50	2
3.	Maximum Data Skew	nSEC	80 *	3
4.	Maximum No. of Stimulus Inputs		23	
5.	Maximum No. of Response Outputs		15	
6.	Programmable Stimulus Voltage Range	VOLTS	+0.0 to +5.0	
7.	Programmable Stimulus Voltage Resolution	VOLTS	0.1	
8.	Programmable Response Voltage Range	VOLTS	+0.0 to +5.0	
9.	Programmable Response Voltage Resolution	VOLTS	0.1	
10.	Logic "One" Voltage Maximum	VOLTS	+5.0	
11.	Logic "One" Voltage Minimum	VOLTS	+2.0	
12.	Logic "Zero" Voltage Maximum	VOLTS	+0.8	
13.	Logic "Zero" Voltage Minimum	VOLTS	+0.0	
14.	Maximum Rise Time	nSEC	100 *	
15.	Maximum Fall Time	nSEC	100 *	
16.	Maximum Input/Output Interface Sink Current	ma	50 *	16
17.	Maximum Input/Output Interface Source Current	ma	50 *	17
18.	Number of Power Supply Voltages Required		2	
19.	Power Supply Voltages	VOLTS	+12.0, +5.0	
20.	Maximum Clock Rate	KHZ	50	20
21.	Serial Data Type		N/A	21
22.	Maximum Serial Stimulus Word Length	BITS	N/A	
23.	Maximum Serial Response Word Length	BITS	N/A	
24.	No. of Bidirectional Lines		16	
25.	Total Used I/O PIN Count		38	
A.	Dynamic Testing		Yes	A
B.	Bidirectional Input/Output		Yes	B
C.	Bidirectional Bus		Yes	C
D.	Serial Node		No	D
E.	Pulse Catch		No	E
F.	Ready/Resume (Handshake)		Yes	F
G.	Architecture Function & Bus Type		Multibus	

PARAMETER		UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
H.	LSI & VLSI Types		1Mbit Bubble	
I.	Microprocessor Type		N/A	
J.	BIT Microprocessor Peripherals		N/A	
K.	Memory Type		Bubble	
L.	Memory Size	BITS	512K x 8	

NOTES:

1. Use logic family names, such as TTL, ECL, CMOS, etc. for the logic the ATE must handle.
2. The maximum data rate in Mb/s that the ATE must supply.
3. The maximum deviation in time between data bits applied synchronously allowed for the ATE.
16. The maximum current ATE driver/receiver must handle to ground in milliamperes (ma).
17. The maximum current ATE driver/receiver must supply in milliamperes (ma).
20. The maximum clock frequency the ATE must supply.
21. The serial data type as RZ or NRZ the ATE must test.

A. A yes indicates that the ATE must test one or more signal properties or characteristics excluding voltage and current.

B,C,D. Enter yes if required.

E. A yes indicates that the ATE must detect and measure a oneshot output.

F. A yes indicates that the ATE must operate in a handshake mode of operation.

N/A Not applicable.

N/S Not specified.

* Estimated.

COMMERCIAL SYSTEM/BOARDS ELECTRONIC TEST EQUIPMENT PARAMETER REQUIREMENTS

System Nomenclature: Disk Memory Set
System/Board Contractor: IBM
Board Nomenclature: MPA1
System/Board Source Document Number: DWG# 2829209 & 2829219

	PARAMETER	UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
1.	Logic Family Types		TTL	1
2.	Maximum Data Rate	Mb/s	N/S	2
3.	Maximum Data Skew	nSEC	100 *	3
4.	Maximum No. of Stimulus Inputs		99	
5.	Maximum No. of Response Outputs		207	
6.	Programmable Stimulus Voltage Range	VOLTS	+0.0 to +5.0	
7.	Programmable Stimulus Voltage Resolution	VOLTS	0.1	
8.	Programmable Response Voltage Range	VOLTS	+0.0 to +5.0	
9.	Programmable Response Voltage Resolution	VOLTS	0.1	
10.	Logic "One" Voltage Maximum	VOLTS	+5.0	
11.	Logic "One" Voltage Minimum	VOLTS	+2.0	
12.	Logic "Zero" Voltage Maximum	VOLTS	+0.8	
13.	Logic "Zero" Voltage Minimum	VOLTS	+0.0	
14.	Maximum Rise Time	nSEC	100 *	
15.	Maximum Fall Time	nSEC	100 *	
16.	Maximum Input/Output Interface Sink Current	ma	50 *	16
17.	Maximum Input/Output Interface Source Current	ma	50 *	17
18.	Number of Power Supply Voltages Required		1	
19.	Power Supply Voltages	VOLTS	+5.0	
20.	Maximum Clock Rate	MHZ	N/S	20
21.	Serial Data Type		None	21
22.	Maximum Serial Stimulus Word Length	BITS	N/A	
23.	Maximum Serial Response Word Length	BITS	N/A	
24.	No. of Bidirectional Lines		75	
25.	Total Used I/O PIN Count		306	
A.	Dynamic Testing		No	A
B.	Bidirectional Input/Output		Yes	B
C.	Bidirectional Bus		No	C
D.	Serial Node		No	D
E.	Pulse Catch		No	E
F.	Ready/Resume (Handshake)		No	F
G.	Architecture Function & Bus Type		None	

PARAMETER		UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
H.	LSI & VLSI Types		None	
I.	Microprocessor Type		None	
J.	BIT Microprocessor Peripherals		None	
K.	Memory Type		None	
L.	Memory Size	BITS	None	

NOTES:

1. Use logic family names, such as TTL, ECL, CMOS, etc. for the logic the ATE must handle.
2. The maximum data rate in Mb/s that the ATE must supply.
3. The maximum deviation in time between data bits applied synchronously allowed for the ATE.
16. The maximum current ATE driver/receiver must handle to ground in milliamperes (ma).
17. The maximum current ATE driver/receiver must supply in milliamperes (ma).
20. The maximum clock frequency the ATE must supply.
21. The serial data type as RZ or NRZ the ATE must test.

A. A yes indicates that the ATE must test one or more signal properties or characteristics excluding voltage and current.

B,C,D. Enter yes if required.

E. A yes indicates that the ATE must detect and measure a oneshot output.

F. A yes indicates that the ATE must operate in a handshake mode of operation.

N/A Not applicable.

N/S Not specified.

* Estimated.

COMMERCIAL SYSTEM/BOARDS ELECTRONIC TEST EQUIPMENT PARAMETER REQUIREMENTS

System Nomenclature: Disk Memory Set
System/Board Contractor: IBM
Board Nomenclature: MPA2
System/Board Source Document Number: DWG# 2828039 & 2828049

	PARAMETER	UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
1.	Logic Family Types		TTL	1
2.	Maximum Data Rate	Mb/s	N/S	2
3.	Maximum Data Skew	nSEC	100 *	3
4.	Maximum No. of Stimulus Inputs		118	
5.	Maximum No. of Response Outputs		163	
6.	Programmable Stimulus Voltage Range	VOLTS	+0.0 to +5.0	
7.	Programmable Stimulus Voltage Resolution	VOLTS	0.1	
8.	Programmable Response Voltage Range	VOLTS	+0.0 to +5.0	
9.	Programmable Response Voltage Resolution	VOLTS	0.1	
10.	Logic "One" Voltage Maximum	VOLTS	+5.0	
11.	Logic "One" Voltage Minimum	VOLTS	+2.0	
12.	Logic "Zero" Voltage Maximum	VOLTS	+0.8	
13.	Logic "Zero" Voltage Minimum	VOLTS	+0.0	
14.	Maximum Rise Time	nSEC	100 *	
15.	Maximum Fall Time	nSEC	100 *	
16.	Maximum Input/Output Interface Sink Current	ma	50 *	16
17.	Maximum Input/Output Interface Source Current	ma	50 *	17
18.	Number of Power Supply Voltages Required		1	
19.	Power Supply Voltages	VOLTS	+5.0	
20.	Maximum Clock Rate	MHZ	N/S	20
21.	Serial Data Type		None	21
22.	Maximum Serial Stimulus Word Length	BITS	N/A	
23.	Maximum Serial Response Word Length	BITS	N/A	
24.	No. of Bidirectional Lines		33	
25.	Total Used I/O PIN Count		281	
A.	Dynamic Testing		No	A
B.	Bidirectional Input/Output		Yes	B
C.	Bidirectional Bus		No	C
D.	Serial Node		No	D
E.	Pulse Catch		No	E
F.	Ready/Resume (Handshake)		No	F
G.	Architecture Function & Bus Type		None	

PARAMETER		UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
H.	LSI & VLSI Types		None	
I.	Microprocessor Type		None	
J.	BIT Microprocessor Peripherals		None	
K.	Memory Type		None	
L.	Memory Size	BITS	None	

NOTES:

1. Use logic family names, such as TTL, ECL, CMOS, etc. for the logic the ATE must handle.
2. The maximum data rate in Mb/s that the ATE must supply.
3. The maximum deviation in time between data bits applied synchronously allowed for the ATE.
16. The maximum current ATE driver/receiver must handle to ground in milliamperes (ma).
17. The maximum current ATE driver/receiver must supply in milliamperes (ma).
20. The maximum clock frequency the ATE must supply.
21. The serial data type as RZ or NRZ the ATE must test.

A. A yes indicates that the ATE must test one or more signal properties or characteristics excluding voltage and current.

B,C,D. Enter yes if required.

E. A yes indicates that the ATE must detect and measure a oneshot output.

F. A yes indicates that the ATE must operate in a handshake mode of operation.

N/A Not applicable.

N/S Not specified.

* Estimated.

COMMERCIAL SYSTEM/BOARDS ELECTRONIC TEST EQUIPMENT PARAMETER REQUIREMENTS

System Nomenclature: Disk Memory Set
System/Board Contractor: IBM
Board Nomenclature: Host Adapter Fast
System/Board Source Document Number: DWG# 2829189 & 2829199

	PARAMETER	UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
1.	Logic Family Types		TTL	1
2.	Maximum Data Rate	Mb/s	N/S	2
3.	Maximum Data Skew	nSEC	100 *	3
4.	Maximum No. of Stimulus Inputs		78	
5.	Maximum No. of Response Outputs		227	
6.	Programmable Stimulus Voltage Range	VOLTS	+0.0 to +5.0	
7.	Programmable Stimulus Voltage Resolution	VOLTS	0.1	
8.	Programmable Response Voltage Range	VOLTS	+0.0 to +5.0	
9.	Programmable Response Voltage Resolution	VOLTS	0.1	
10.	Logic "One" Voltage Maximum	VOLTS	+5.0	
11.	Logic "One" Voltage Minimum	VOLTS	+2.0	
12.	Logic "Zero" Voltage Maximum	VOLTS	+0.8	
13.	Logic "Zero" Voltage Minimum	VOLTS	+0.0	
14.	Maximum Rise Time	nSEC	100 *	
15.	Maximum Fall Time	nSEC	100 *	
16.	Maximum Input/Output Interface Sink Current	ma	50 *	16
17.	Maximum Input/Output Interface Source Current	ma	50 *	17
18.	Number of Power Supply Voltages Required		1	
19.	Power Supply Voltages	VOLTS	+5.0	
20.	Maximum Clock Rate	MHZ	N/S	20
21.	Serial Data Type		None	21
22.	Maximum Serial Stimulus Word Length	BITS	N/A	
23.	Maximum Serial Response Word Length	BITS	N/A	
24.	No. of Bidirectional Lines		44	
25.	Total Used I/O PIN Count		305	
A.	Dynamic Testing		No	A
B.	Bidirectional Input/Output		Yes	B
C.	Bidirectional Bus		No	C
D.	Serial Node		No	D
E.	Pulse Catch		No	E
F.	Ready/Resume (Handshake)		No	F
G.	Architecture Function & Bus Type		None	

PARAMETER		UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
H.	LSI & VLSI Types		None	
I.	Microprocessor Type		None	
J.	BIT Microprocessor Peripherals		None	
K.	Memory Type		None	
L.	Memory Size	BITS	None	

NOTES:

1. Use logic family names, such as TTL, ECL, CMOS, etc. for the logic the ATE must handle.
2. The maximum data rate in Mb/s that the ATE must supply.
3. The maximum deviation in time between data bits applied synchronously allowed for the ATE.
16. The maximum current ATE driver/receiver must handle to ground in milliamperes (ma).
17. The maximum current ATE driver/receiver must supply in milliamperes (ma).
20. The maximum clock frequency the ATE must supply.
21. The serial data type as RZ or NRZ the ATE must test.

A. A yes indicates that the ATE must test one or more signal properties or characteristics excluding voltage and current.

B,C,D. Enter yes if required.

E. A yes indicates that the ATE must detect and measure a oneshot output.

F. A yes indicates that the ATE must operate in a handshake mode of operation.

N/A Not applicable.

N/S Not specified.

* Estimated.

COMMERCIAL SYSTEM/BOARDS ELECTRONIC TEST EQUIPMENT PARAMETER REQUIREMENTS

System Nomenclature: Disk Memory Set
System/Board Contractor: IBM
Board Nomenclature: Host Adapter Slow
System/Board Source Document Number: DWG# 2827979 & 2827989

	PARAMETER	UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
1.	Logic Family Types		TTL	1
2.	Maximum Data Rate	Mb/s	N/S	2
3.	Maximum Data Skew	nSEC	100 *	3
4.	Maximum No. of Stimulus Inputs		78	
5.	Maximum No. of Response Outputs		229	
6.	Programmable Stimulus Voltage Range	VOLTS	+0.0 to +5.0	
7.	Programmable Stimulus Voltage Resolution	VOLTS	0.1	
8.	Programmable Response Voltage Range	VOLTS	+0.0 to +5.0	
9.	Programmable Response Voltage Resolution	VOLTS	0.1	
10.	Logic "One" Voltage Maximum	VOLTS	+5.0	
11.	Logic "One" Voltage Minimum	VOLTS	+2.0	
12.	Logic "Zero" Voltage Maximum	VOLTS	+0.8	
13.	Logic "Zero" Voltage Minimum	VOLTS	+0.0	
14.	Maximum Rise Time	nSEC	100 *	
15.	Maximum Fall Time	nSEC	100 *	
16.	Maximum Input/Output Interface Sink Current	ma	50 *	16
17.	Maximum Input/Output Interface Source Current	ma	50 *	17
18.	Number of Power Supply Voltages Required		1	
19.	Power Supply Voltages	VOLTS	+5.0	
20.	Maximum Clock Rate	MHZ	N/S	20
21.	Serial Data Type		None	21
22.	Maximum Serial Stimulus Word Length	BITS	N/A	
23.	Maximum Serial Response Word Length	BITS	N/A	
24.	No. of Bidirectional Lines		95	
25.	Total Used I/O PIN Count		307	
A.	Dynamic Testing		No	A
B.	Bidirectional Input/Output		Yes	B
C.	Bidirectional Bus		No	C
D.	Serial Node		No	D
E.	Pulse Catch		No	E
F.	Ready/Resume (Handshake)		No	F
G.	Architecture Function & Bus Type		None	

PARAMETER		UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
H.	LSI & VLSI Types		None	
I.	Microprocessor Type		None	
J.	BIT Microprocessor Peripherals		None	
K.	Memory Type		None	
L.	Memory Size	BITS	None	

NOTES:

1. Use logic family names, such as TTL, ECL, CMOS, etc. for the logic the ATE must handle.
2. The maximum data rate in Mb/s that the ATE must supply.
3. The maximum deviation in time between data bits applied synchronously allowed for the ATE.
16. The maximum current ATE driver/receiver must handle to ground in milliamperes (ma).
17. The maximum current ATE driver/receiver must supply in milliamperes (ma).
20. The maximum clock frequency the ATE must supply.
21. The serial data type as RZ or NRZ the ATE must test.

A. A yes indicates that the ATE must test one or more signal properties or characteristics excluding voltage and current.

B,C,D. Enter yes if required.

E. A yes indicates that the ATE must detect and measure a oneshot output.

F. A yes indicates that the ATE must operate in a handshake mode of operation.

N/A Not applicable.

N/S Not specified.

* Estimated.

COMMERCIAL SYSTEM/BOARDS ELECTRONIC TEST EQUIPMENT PARAMETER REQUIREMENTS

System Nomenclature: Disk Memory Set
System/Board Contractor: IBM
Board Nomenclature: Read/Write Control
System/Board Source Document Number: DWG# 2829249 & 282959

	PARAMETER	UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
1.	Logic Family Types		TTL	1
2.	Maximum Data Rate	Mb/s	N/S	2
3.	Maximum Data Skew	nSEC	100 *	3
4.	Maximum No. of Stimulus Inputs		85	
5.	Maximum No. of Response Outputs		156	
6.	Programmable Stimulus Voltage Range	VOLTS	+0.0 to +5.0	
7.	Programmable Stimulus Voltage Resolution	VOLTS	0.1	
8.	Programmable Response Voltage Range	VOLTS	+0.0 to +5.0	
9.	Programmable Response Voltage Resolution	VOLTS	0.1	
10.	Logic "One" Voltage Maximum	VOLTS	+5.0	
11.	Logic "One" Voltage Minimum	VOLTS	+2.0	
12.	Logic "Zero" Voltage Maximum	VOLTS	+0.8	
13.	Logic "Zero" Voltage Minimum	VOLTS	+0.0	
14.	Maximum Rise Time	nSEC	100 *	
15.	Maximum Fall Time	nSEC	100 *	
16.	Maximum Input/Output Interface Sink Current	ma	50 *	16
17.	Maximum Input/Output Interface Source Current	ma	50 *	17
18.	Number of Power Supply Voltages Required		1	
19.	Power Supply Voltages	VOLTS	+5.0	
20.	Maximum Clock Rate	MHZ	N/S	20
21.	Serial Data Type		None	21
22.	Maximum Serial Stimulus Word Length	BITS	N/A	
23.	Maximum Serial Response Word Length	BITS	N/A	
24.	No. of Bidirectional Lines		104	
25.	Total Used I/O PIN Count		241	
A.	Dynamic Testing		No	A
B.	Bidirectional Input/Output		Yes	B
C.	Bidirectional Bus		No	C
D.	Serial Node		No	D
E.	Pulse Catch		No	E
F.	Ready/Resume (Handshake)		No	F
G.	Architecture Function & Bus Type		None	

PARAMETER		UNITS	SYSTEM/BOARD PARAMETER VALUE	NOTES
H.	LSI & VLSI Types		None	
I.	Microprocessor Type		None	
J.	BIT Microprocessor Peripherals		None	
K.	Memory Type		None	
L.	Memory Size	BITS	None	

NOTES:

1. Use logic family names, such as TTL, ECL, CMOS, etc. for the logic the ATE must handle.
2. The maximum data rate in Mb/s that the ATE must supply.
3. The maximum deviation in time between data bits applied synchronously allowed for the ATE.
16. The maximum current ATE driver/receiver must handle to ground in milliamperes (ma).
17. The maximum current ATE driver/receiver must supply in milliamperes (ma).
20. The maximum clock frequency the ATE must supply.
21. The serial data type as RZ or NRZ the ATE must test.

A. A yes indicates that the ATE must test one or more signal properties or characteristics excluding voltage and current.

B,C,D. Enter yes if required.

E. A yes indicates that the ATE must detect and measure a oneshot output.

F. A yes indicates that the ATE must operate in a handshake mode of operation.

N/A Not applicable.

N/S Not specified.

* Estimated.

APPENDIX C

MCF Specification Data

A. Specifications for the AN/UYK-41 Super Minicomputer (CR-CS-0034-002).

Has Central Processor Unit (CPU) and Input/Output (I/O) Processor.

CPU Execution Rate: 3 MIPS without I/O goal
2 MIPS with I/O goal

The CPU shall execute the MIL-STD-1862 Instruction Set Architecture.

CPU Word Size: 32 bits

CPU Clock Frequency: Technology Dependent (in the order of 25 MHz)

Memory:

a. RAM Memory: 4 megabytes minimum
8 megabytes goal

b. EAROM Memory: 128 kilobytes minimum
512 kilobytes goal

(EAROM = Electrically Alterable Read Only Memory)

I/O Processor: Must support an aggregate I/O throughput of at least 6 megabytes/second.

I/O Interface Buses: 2 ea Serial Digital Bus Interfaces
2 ea Parallel Digital Bus Interfaces
2 ea Serial Digital Point to Point Interfaces

Serial Digital Bus Interface: MIL-STD-1553B

Maximum Frequency: 1 megabit/sec

Parallel Digital Bus Interface (CR-CI-004-100):

Data Rate: 2 megabytes/sec 10 meter cable
600 kilobytes/sec 100 meter cable

Interface Requires: 27 Differential Tri-State Driver/Receiver Pairs

Logic: Biphase (Signal Phase determines logic level)

Logic Voltage Magnitude: 2 to 5 volts for both Logic One and Logic Zero

Serial Digital Point to Point Interface (CR-CI-0038-001):

Data Rate: Programmable from 75 baud to 19.2 Kilobaud

Interfaces to: RS-232, RS-449 and AN/UG7-74 teletypewriter

Utilizes a maximum of 10 twisted pair signal lines, can be configured for either RS-232, RS-449 or AN/UG7-74 teletypewriter by cable connector and adaptor.

Constructed with VLSI, technology either CMOS, CMOS/SOS, or bipolar.

Electrical Power Interface: Nominal 28 VDC vehicular power source, MIL-STD-1275 Nominal 115/230 volt 50/60 hertz single phase, type 1, DOD-STD-1399, Sec 300 Nominal 115 volt, 400 hertz, single phase aircraft power source, MIL-STD-704.

B. **Specifications for the AN/UYK-49, MCF Microcomputer (CR-CS-0035-002).**

Has Central Processor Unit (CPU) and I/O Processor.

CPU Execution Rate:	500 KIPS	without I/O	goal
	300 KIPS	with I/O	goal

*Note: With I/O: with each high speed parallel digital Data Bus Interface transferring data to or from memory at a total rate of 500 kilobytes/sec.

CPU Word Size: 32 bits

CPU Clock Frequency: Technology Dependent (in the order of 6 MHz)

CPU Must Execute: MIL-STD-1862 Instruction Set Architecture (Nebula).

Memory:

a. RAM Memory: 4 megabytes minimum
8 megabytes goal

b. EAROM Memory: 128 kilobytes minimum
512 kilobytes goal

(EAROM = Electrically Alterable Read Only Memory)

I/O Processor: Must support an aggregate I/O throughput of 2 megabytes/second.

I/O Interface Buses: 2 ea Serial Digital Bus Interfaces (MIL-STD-1553B) -
1 megabit/sec data rate
2 ea Serial Digital Point to Point Interfaces (RS 232, RS 449) -
max data rate 19.2 kiloboud
2 ea Parallel Digital Bus Interfaces -
max data rate 2 megabytes/sec

Power Source: 28 VDC vehicular

Nominal 115/230 volt, 50/60 hertz, single phase

Nominal 115 volt, 400 hertz, single phase aircraft supply.

C. **Specifications for the NCF Single Module Computer Available Data (CR-CS-0086-01) (under development).**

CPU Data Rate: 500 KIPS goal

CPU Work Size: 32 bits

CPU Clock Frequency: Technology Dependent (in the order of 6 MHz)

Self Contained RAM Memory: 256 kilobytes

External Memory Addressing Capability: 8 megabytes via separate address and data lines

Single Module Computer Interfaces: (1) Memory Interface, (2) Processor Control and Status Bus Interface, and (3) Power Interface.

CPU Performance Requirements: Must execute MIL-STD-1862 Nebula Instruction Set Architecture

Construction With: VLSI; technology either CMOS, CMOS/SOS, bipolar

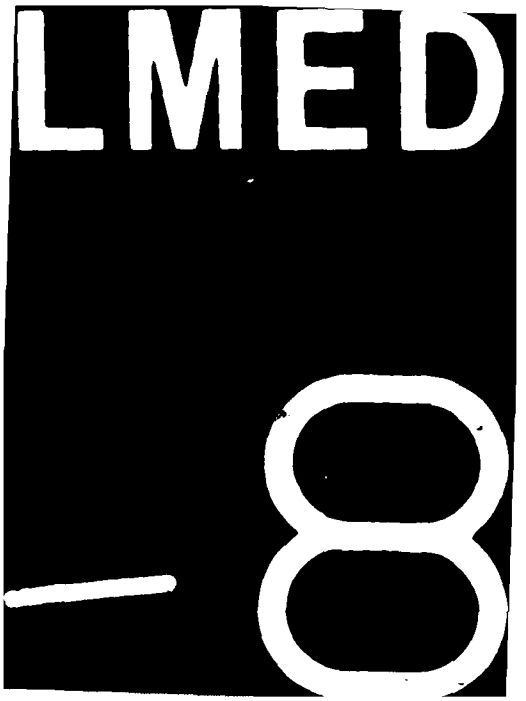
Electrical Power Sources: Nominal 28V DC vehicular power source
Nominal 115/230 volt, 50/60 hertz, single phase
Nominal 115 volt, 400 hertz, single phase aircraft power source

APPENDIX D

Acronyms and Abbreviations

ATE	Automatic Test Equipment
baud	Binary Units of Information Per Second
Bits	Binary Digits
bps	Bits per Second
byte	A group of eight (8) binary digits
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
DRAM	Dynamic Random Access Memory
EAROM	Electrically Alterable Read Only Memory
ECL	Emitter-Coupled Logic
est.	Estimated
FIFO	First in, First out
HMOS	High Performance Metal Oxide Semiconductor
HTL	High Threshold Logic
K	Kilo or Thousand
Kb/s	Kilobits per Second
KIPS	Kilo-instruction per Second
LSI	Large Scale Integration
M	Mega or Million
ma	Milliampere
Mb/s	Megabits per Second
MCF	Military Computer Family
MIPS	Million Instruction per Second
uSec	Microsecond
MLRS	Multiple Launch Rocket System
MOS	Metal Oxide Semiconductor
msec	Millesecond
N/A	Not Applicable
NMOS	N-Type Metal Oxide Semiconductor
NRZ	Nonreturn to Zero
N/S	Not Specified
nSec	Nanosecond
NTDS	Naval Tactical Data System
PROM	Programmable Read-Only Memory
RAM	Random Access Memory
Resp	Response

ROM	Read-Only Memory
RZ	Return to Zero
SEC	Second
Stim	Stimulus
TTL	Transistor-Transister Logic
UART	Universal Asynchronous Receiver Transmitter
VLSI	Very Large Scale Integration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